

Compal Confidential

L380 / Y580S

M/B Schematic Document

AMD Phoenix Processor with DDR5 SO- DIMM

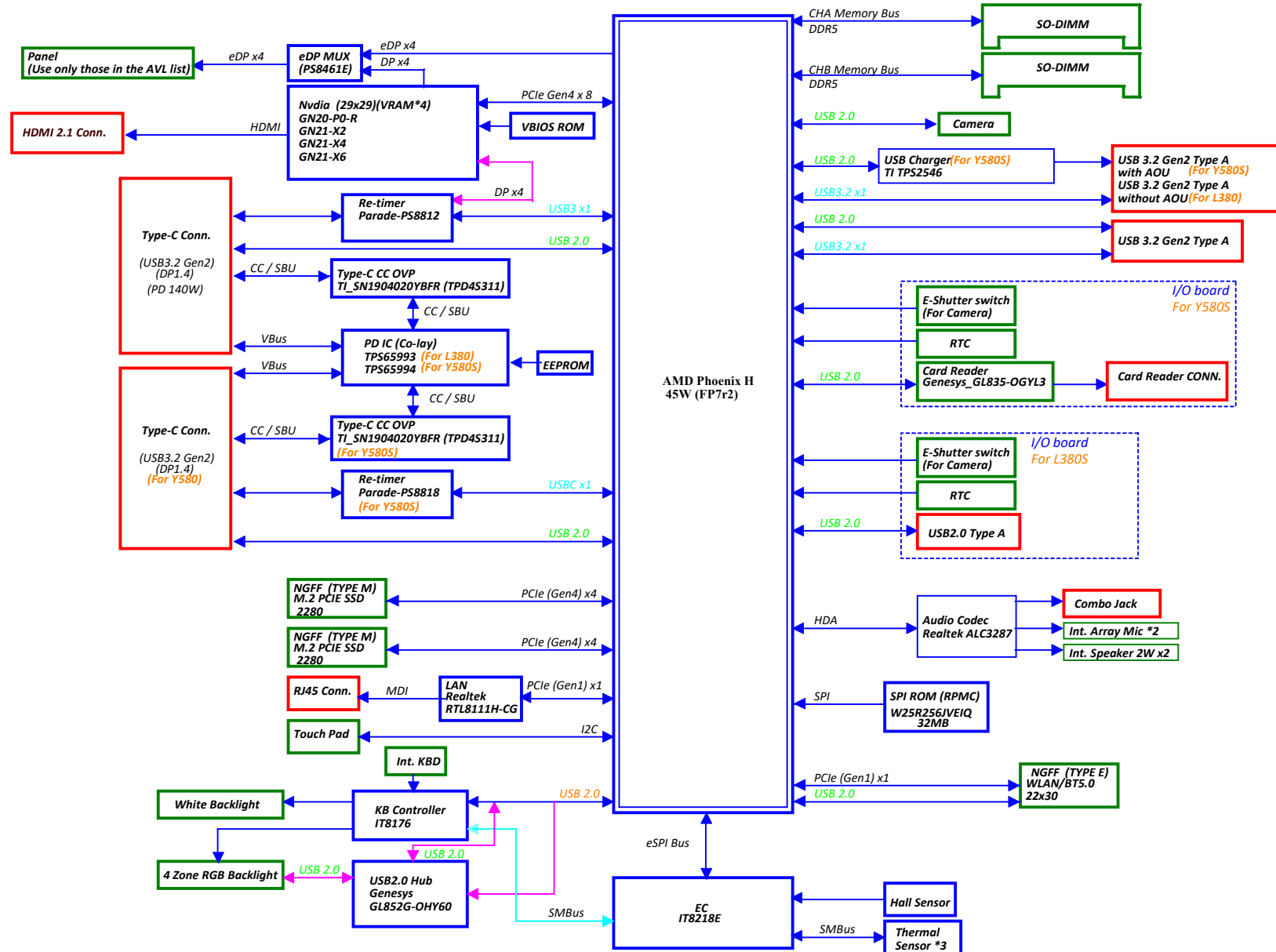
2023-02-16

LA-M811P

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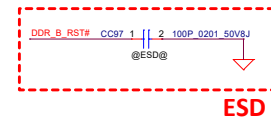
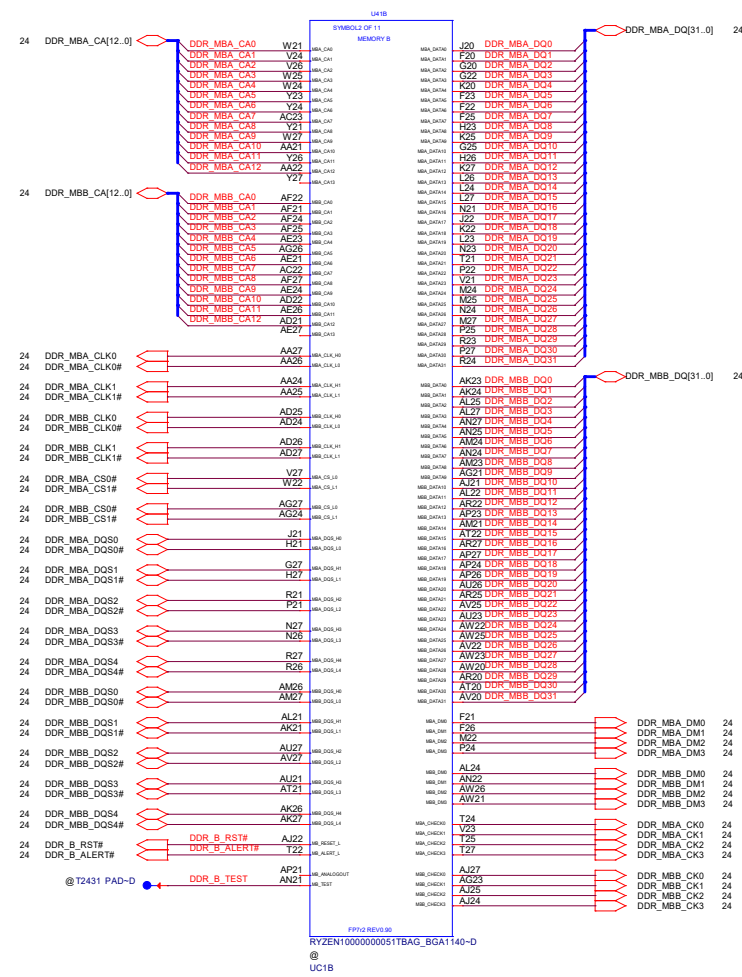
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AMD Phoenix Block Diagram



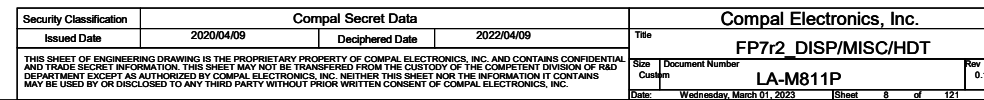
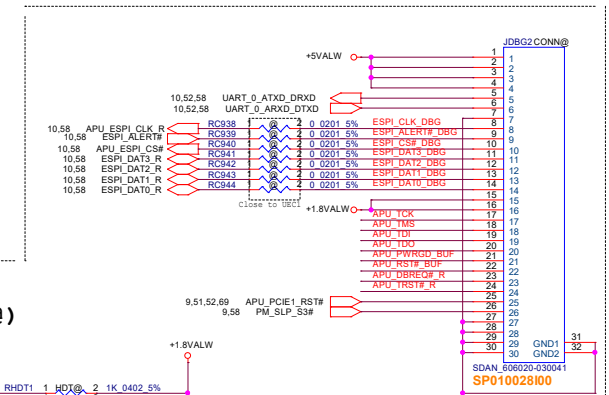
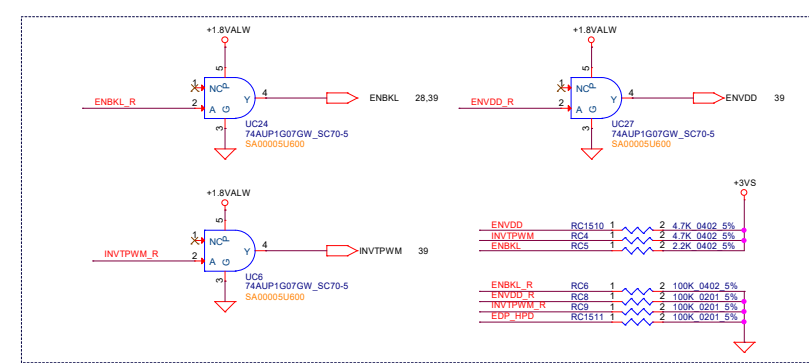
PCB BOARD SIZE	
mm	X mm
10 Layer	
 	Internal Slot/Header
 	Front/Rear IO
 	Chipset
 	Optional

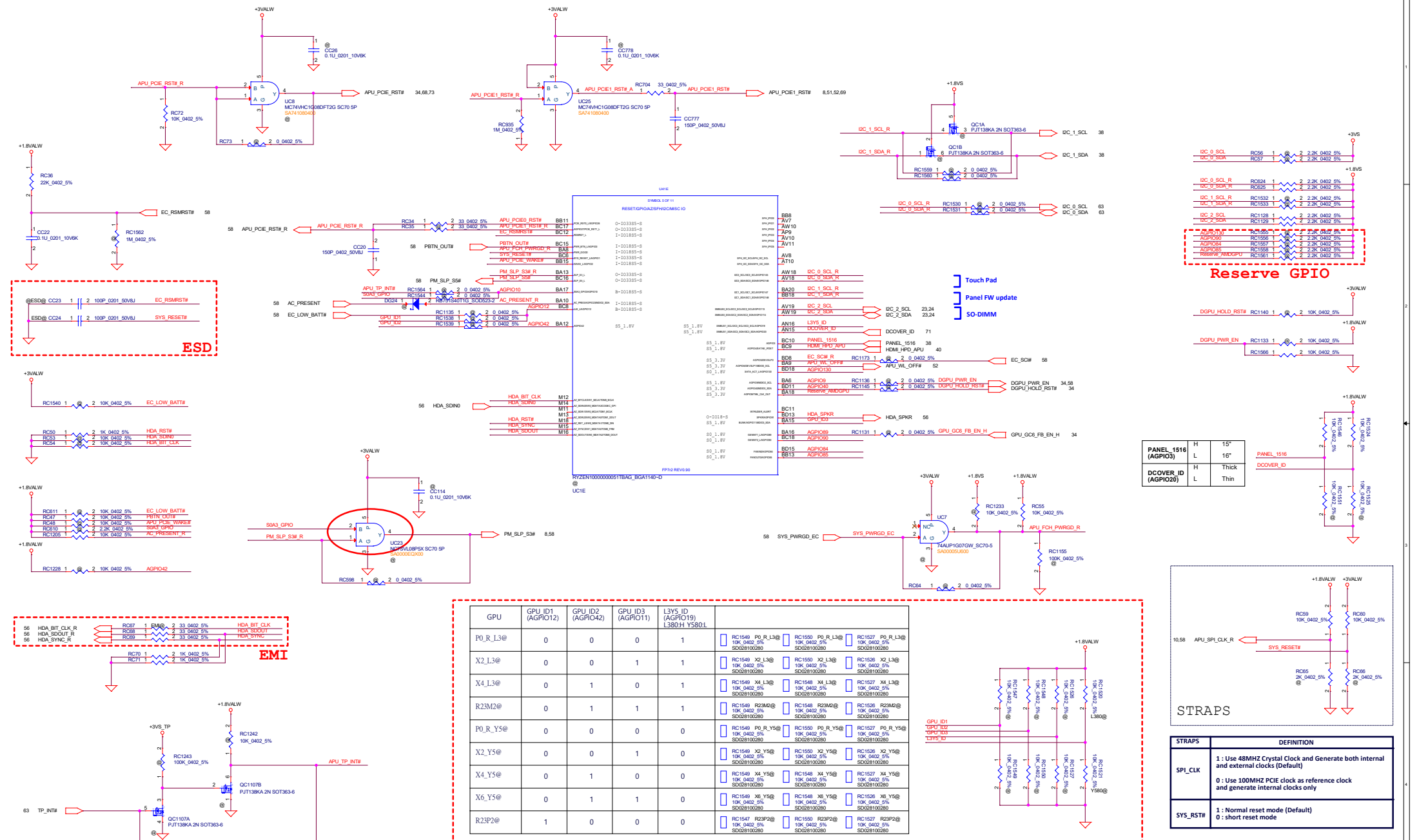
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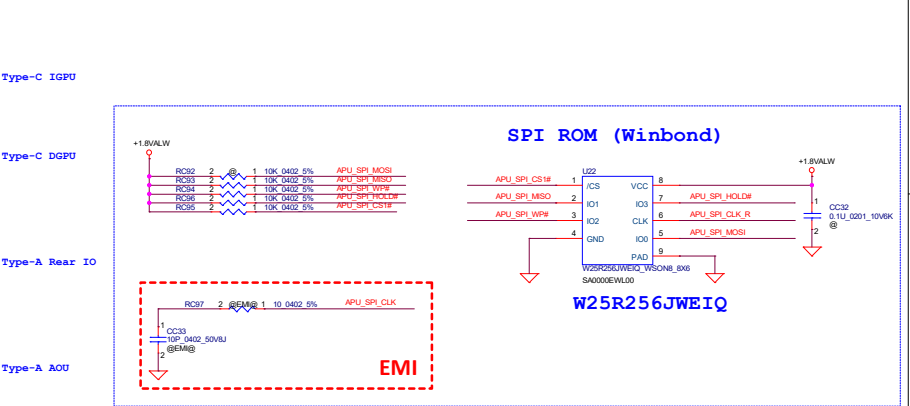
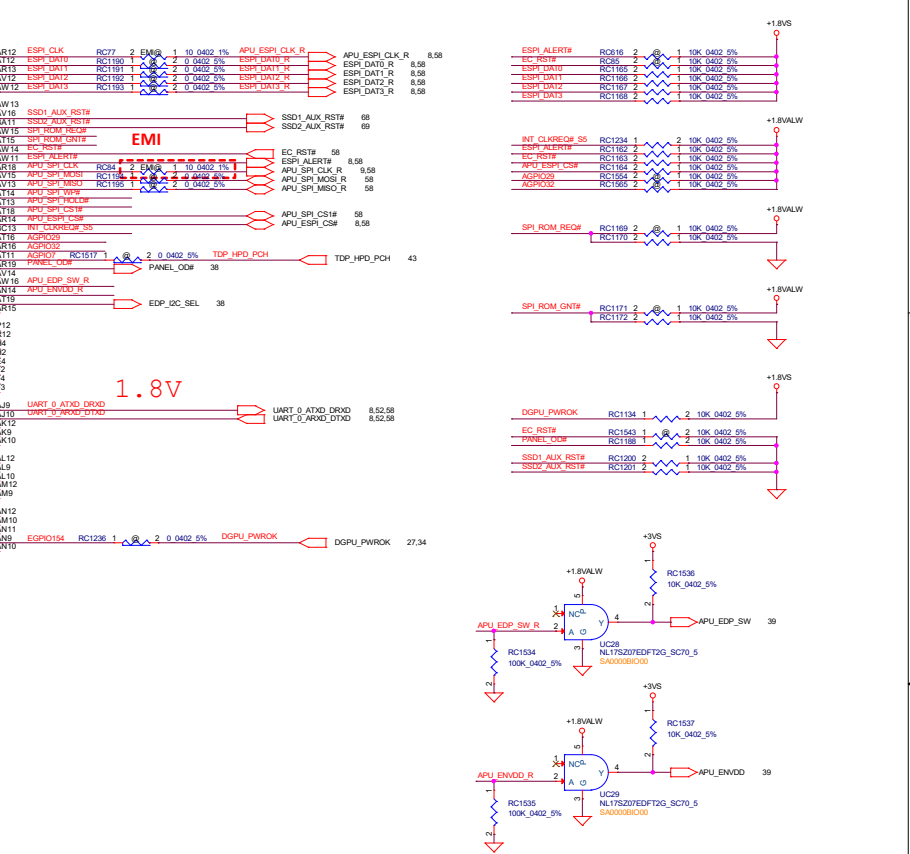
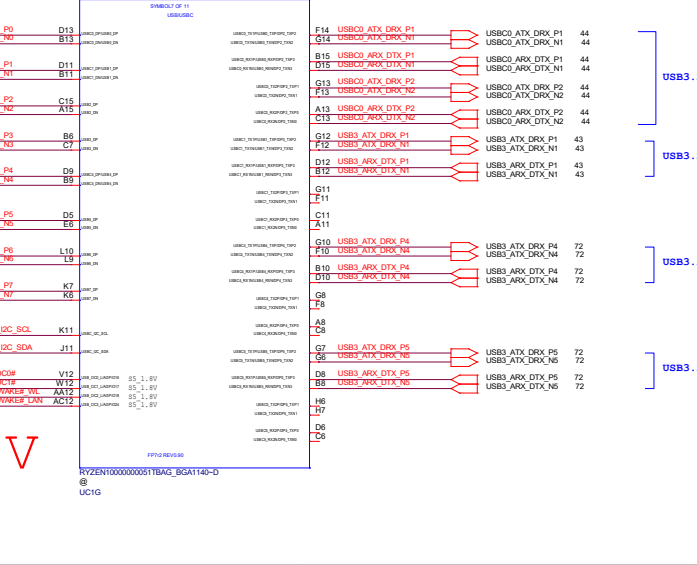
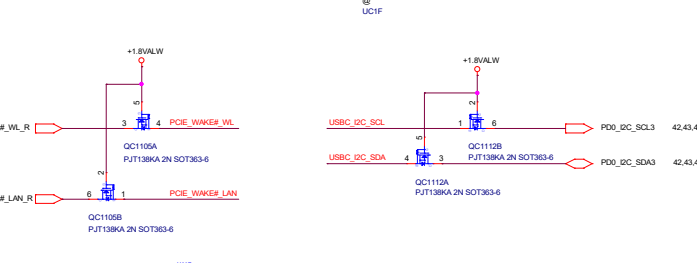
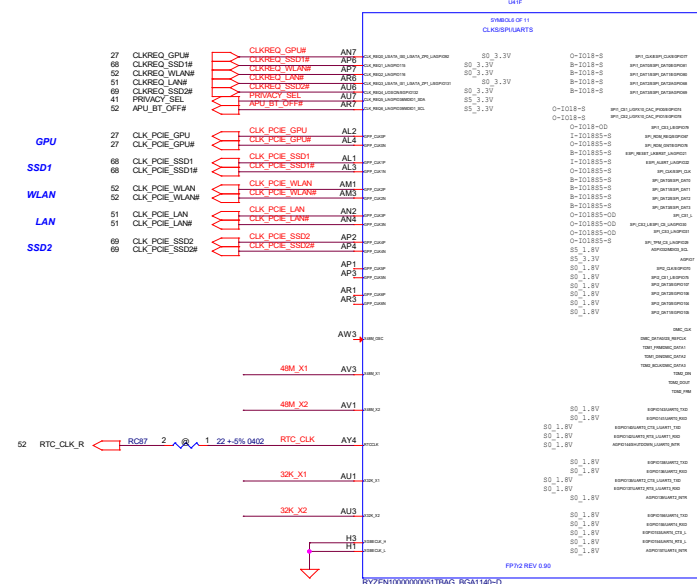
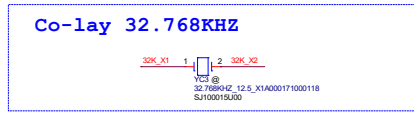
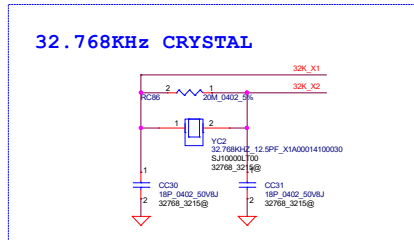
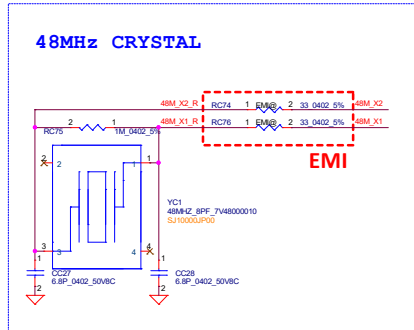
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Issued Date	2020/04/09	Deciphered Date	2022/04/09	Title	F7P7r DDR5 MEMORY I/F
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DP0: eDP
DP1: HDMI
DP2: Type-C
DP3: N/A
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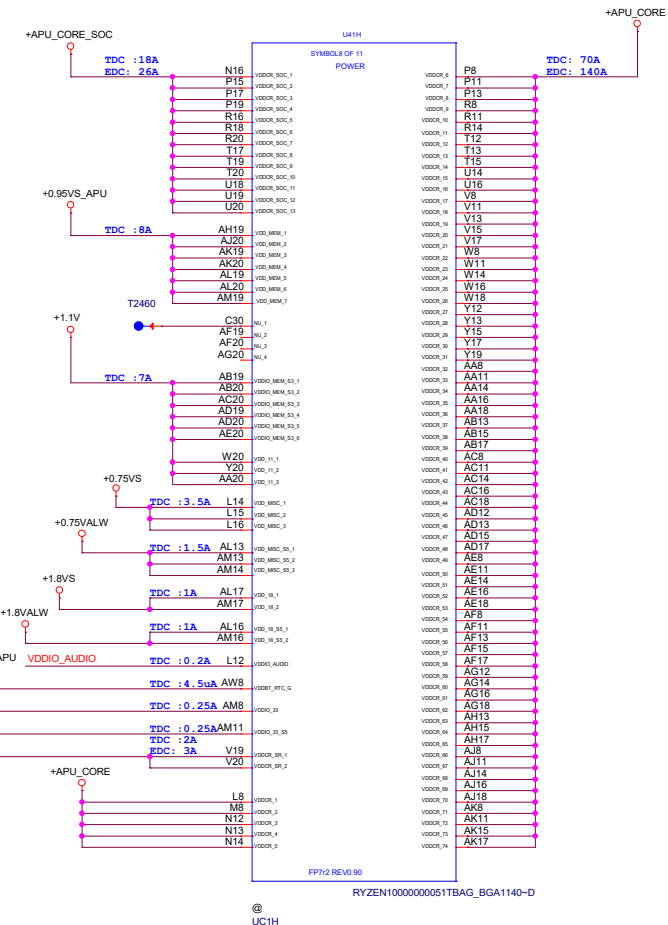
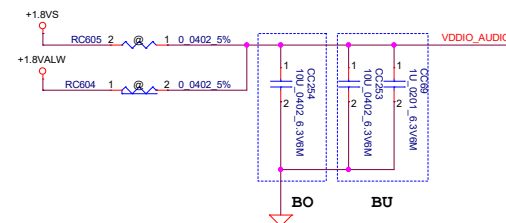
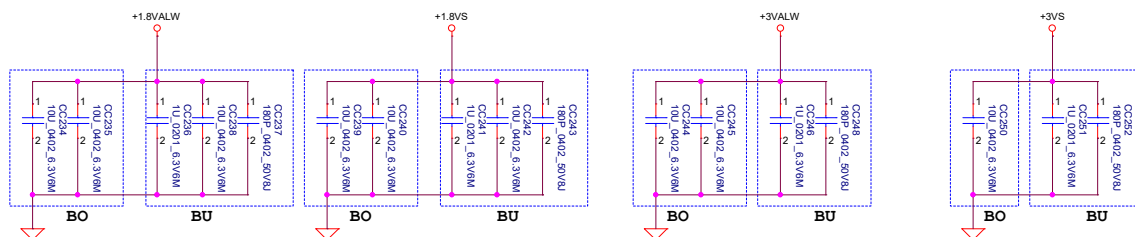




GPU	GPU_ID1 (AGPIO12)	GPU_ID2 (AGPIO42)	GPU_ID3 (AGPIO11)	L3Y5_ID (AGPIO19) L380 H Y580 L
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X2_L3@	0	0	1	1
X4_L3@	0	1	0	1
R23M2@	0	1	1	1
P0_R_Y5@	0	0	0	0
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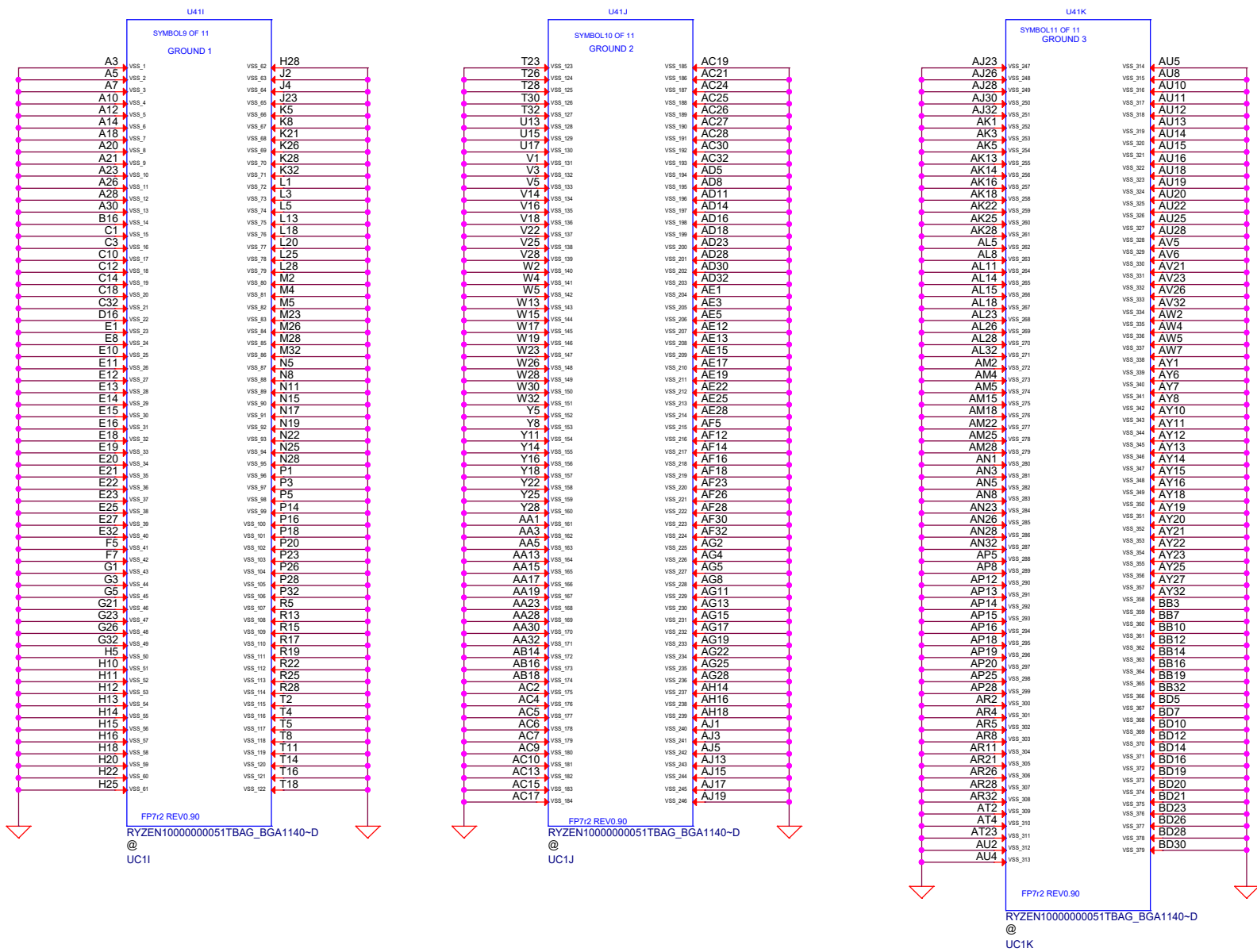


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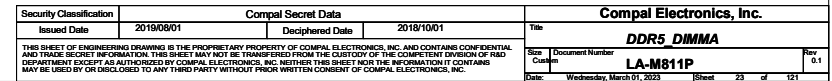
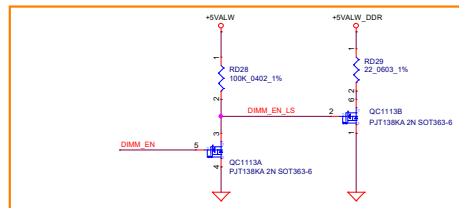
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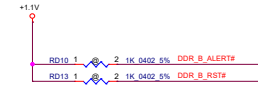
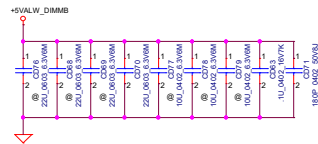
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Main Func = CPU



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6	DDR_MBA_DQ73	200	CA12_V	200	RFL71	200	HSA	75	RD1 1	2	15.4K 0402 1%	200	DDR_MBA_DQ73	6
6	DDR_MBA_DQ74	201	CA12_W	201	RFL72	201	HSA	76	RD1 1	2	15.4K 0402 1%	201	DDR_MBA_DQ74	6
6	DDR_MBA_DQ75	202	CA12_X	202	RFL73	202	HSA	77	RD1 1	2	15.4K 0402 1%	202	DDR_MBA_DQ75	6
6	DDR_MBA_DQ76	203	CA12_Y	203	RFL74	203	HSA	78	RD1 1	2	15.4K 0402 1%	203	DDR_MBA_DQ76	6
6	DDR_MBA_DQ77	204	CA12_Z	204	RFL75	204	HSA	79	RD1 1	2	15.4K 0402 1%	204	DDR_MBA_DQ77	6
6	DDR_MBA_DQ78	205	CA12_A	205	RFL76	205	HSA	80	RD1 1	2	15.4K 0402 1%	205	DDR_MBA_DQ78	6
6	DDR_MBA_DQ79	206	CA12_B	206	RFL77	206	HSA	81	RD1 1	2	15.4K 0402 1%	206	DDR_MBA_DQ79	6
6	DDR_MBA_DQ80	207	CA12_C	207	RFL78	207	HSA	82	RD1 1	2	15.4K 0402 1%	207	DDR_MBA_DQ80	6
6	DDR_MBA_DQ81	208	CA12_D	208	RFL79	208	HSA	83	RD1 1	2	15.4K 0402 1%	208	DDR_MBA_DQ81	6
6	DDR_MBA_DQ82	209	CA12_E	209	RFL80	209	HSA	84	RD1 1	2	15.4K 0402 1%	209	DDR_MBA_DQ82	6
6	DDR_MBA_DQ83	210	CA12_F	210	RFL81	210	HSA	85	RD1 1	2	15.4K 0402 1%	210	DDR_MBA_DQ83	6
6	DDR_MBA_DQ84	211	CA12_G	211	RFL82	211	HSA	86	RD1 1	2	15.4K 0402 1%	211	DDR_MBA_DQ84	6
6	DDR_MBA_DQ85	212	CA12_H	212	RFL83	212	HSA	87	RD1 1	2	15.4K 0402 1%	212	DDR_MBA_DQ85	6
6	DDR_MBA_DQ86	213	CA12_I	213	RFL84	213	HSA	88	RD1 1	2	15.4K 0402 1%	213	DDR_MBA_DQ86	6
6	DDR_MBA_DQ87	214												

GC OFF 1.0 GPU Power ON/OFF

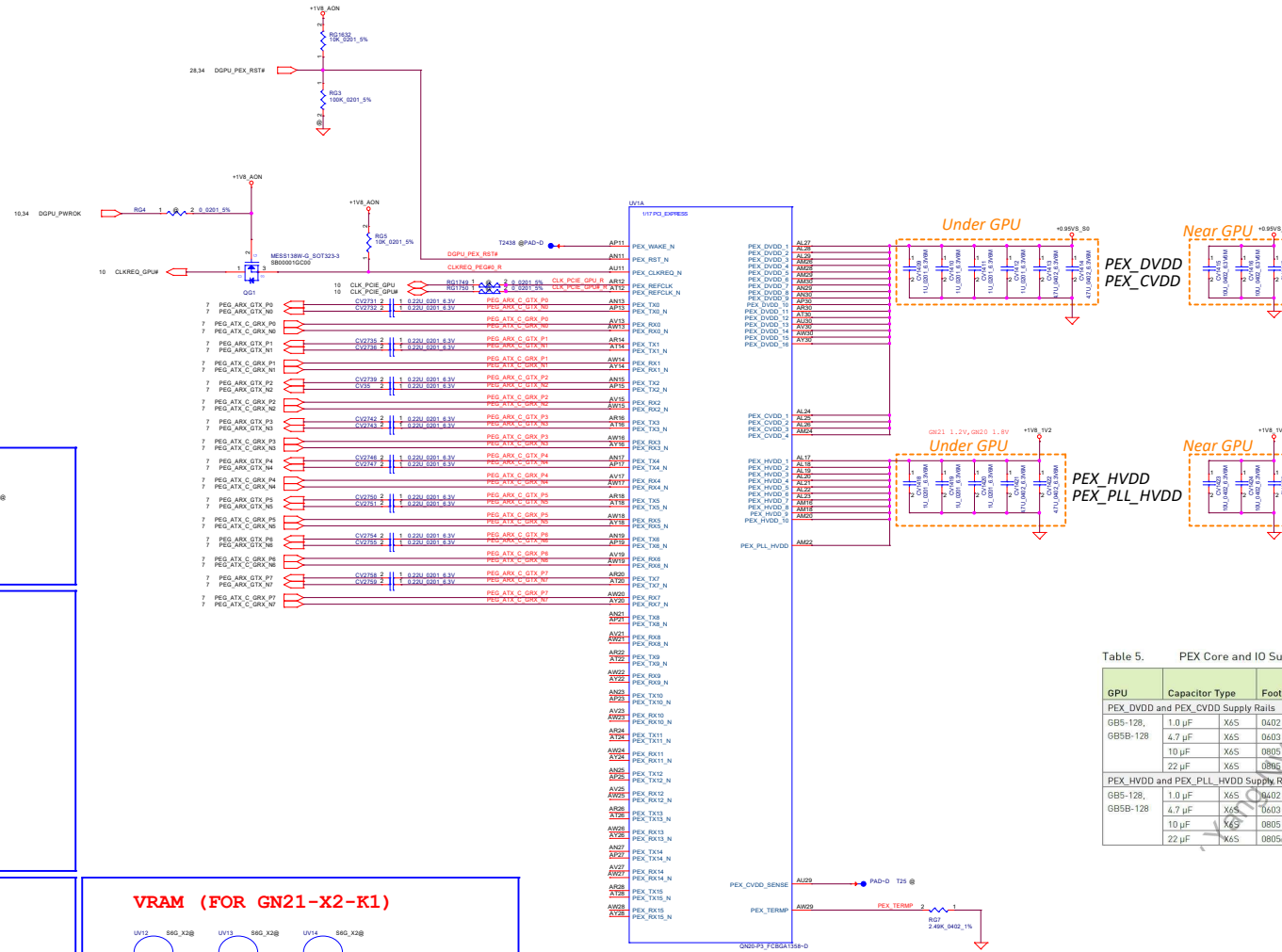
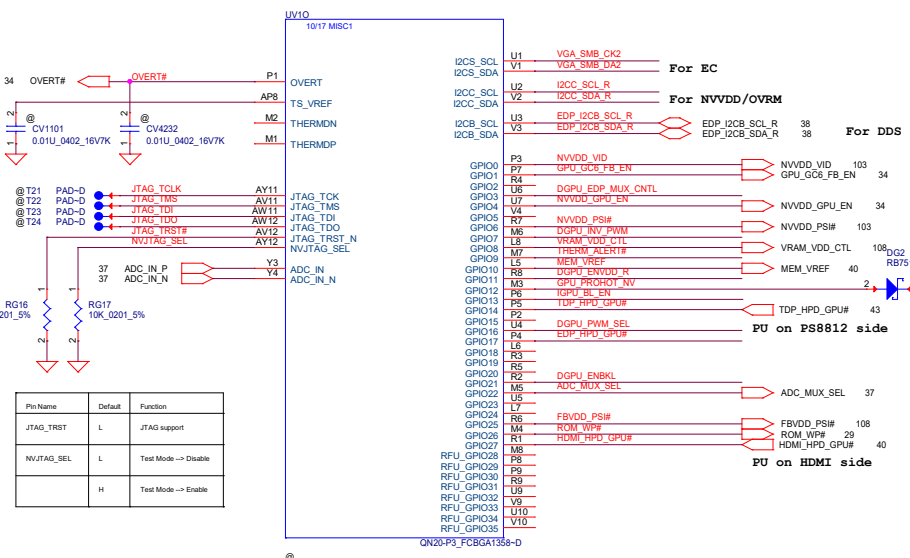


Table 5. PEX Core and IO Supply Decoupling and Filtering

GPU		Capacitor Type	Footprint	Population		Location
				GB5-128	GB5B-128	
PEX_DVDD and PEX_CVDD Supply Rails						
GB5-128, GB5B-128	1.0 μ F	X65	0402 or 0201W	4	2	Under GPU
	4.7 μ F	X65	0603	2	2	Under GPU
	10 μ F	X65	0805	2	2	Near GPU
	22 μ F	X65	0806	1	1	Near GPU
PEX_HVDD and PEX_PLL_HVDD Supply Rails						
GB5-128, GB5B-128	1.0 μ F	X65	0402 or 0201W	3	3	Under GPU
	4.7 μ F	X65	0603	2	2	Under GPU
	10 μ F	X65	0805	2	2	Near GPU
	22 μ F	X65	0805	1	1	Near GPU



Pin Name	Default	Function
JTAG_TRST	L	JTAG support
NVJTAG_SEL	L	Test Mode -> Disable
	H	Test Mode -> Enable

AMD MS change to 3VALW

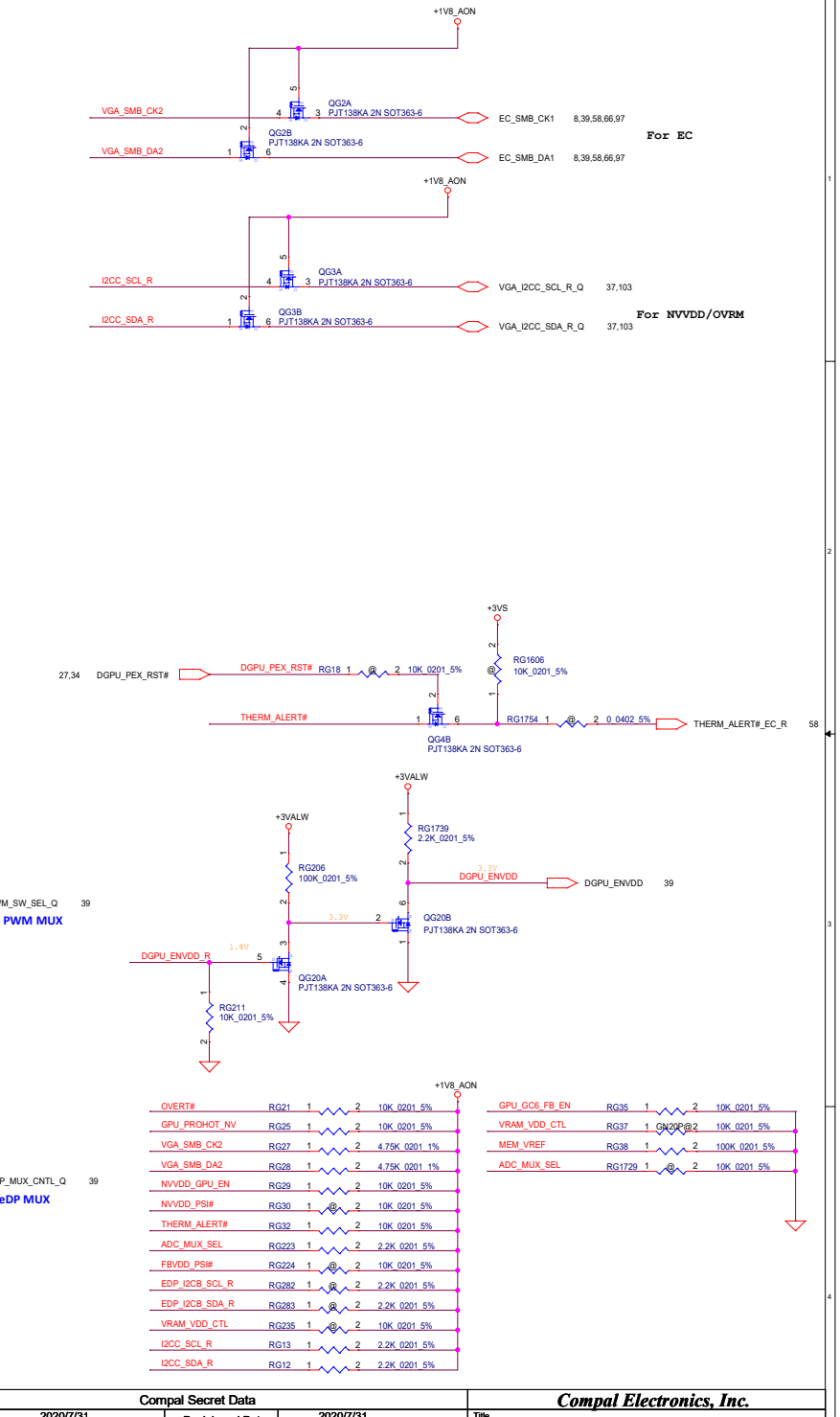
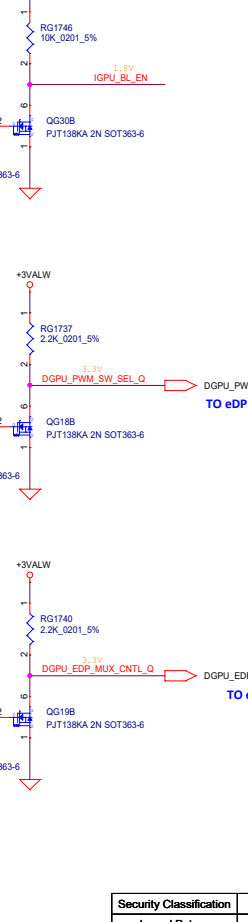
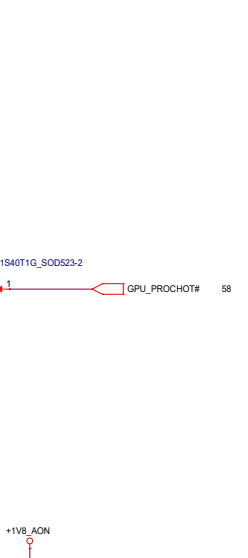
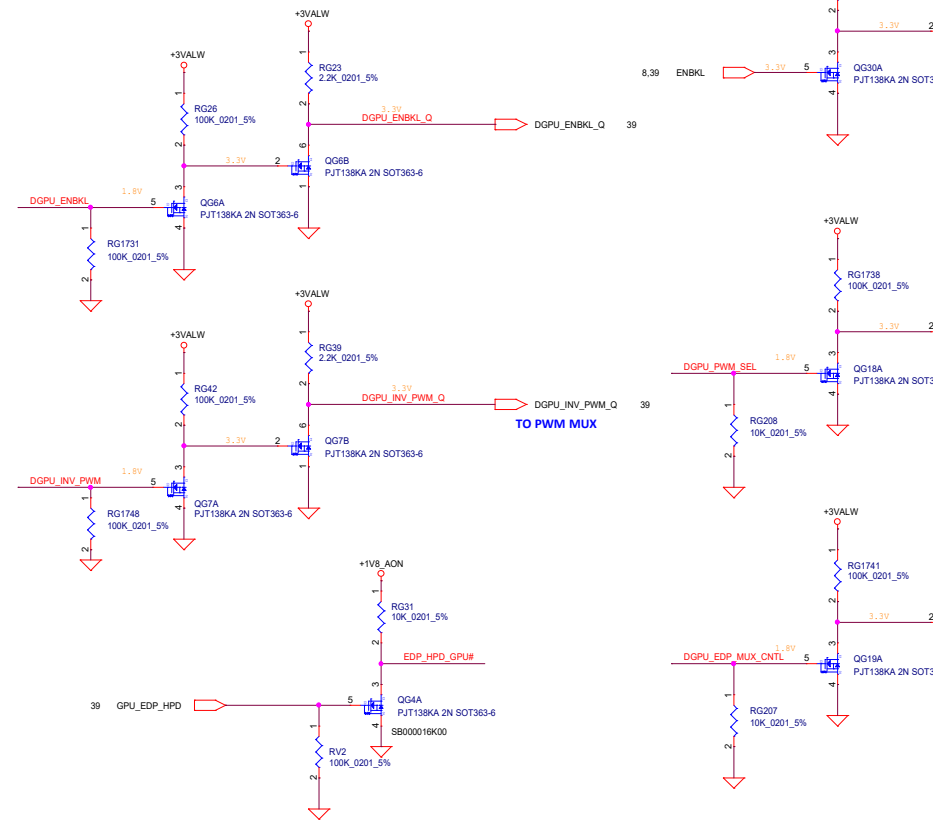


Table 7-3. RAMCFG

Strap Pins ¹			RAMCFG Setting Number	
Strap2	Strap1	Strap0	For Down-Design, see Memory RVL for memory configs corresponding to these numbers.	
L	L	L	0	0x0000
L	L	M	1	0x0001
L	L	H	2	0x0002
L	M	L	3	0x0003
L	M	M	4	0x0004
L	M	H	5	0x0005
L	H	L	6	0x0006
L	H	M	7	0x0007
L	H	H	8	0x0008
M	L	L	9	0x0009
M	L	M	10	0x000A
M	L	H	11	0x000B
M	M	L	12	0x000C
M	M	M	13	0x000D
M	M	H	14	0x000E
M	H	L	15	0x000F
M	H	M	16	0x0010
M	H	H	17	0x0011
H	L	L	18	0x0012
H	L	M	19	0x0013
H	L	H	20	0x0014
H	M	L	21	0x0015
H	M	M	22	0x0016
H	M	H	23	0x0017
H	H	L	24	0x0018
H	H	M	25	0x0019
H	H	H	26	0x001A

Note¹: The ternary strap pins listed in the STRAP columns must be pulled to one of three voltage levels. "L" means Low level (0.9V), "M" means Middle level (0.9V), "H" means High level (1.8V).

Table 6. GN20-P0-R-K2 GDDR6 Recommended Memories

Memory Density	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Support GPU Min/Max
16Gb	20h513M16	1.2V 1.2V	Samsung	K4ZAF328C-SC16	A-die	16 Gbps	2216	Full	Production candidate	PS or later
			Hynix	H56G4254D014	A-die	16 Gbps	2216	Full	Production candidate	PS or later
			Micron	MT61K032M28P9A-16C	C-die	16 Gbps	2216	Full	Production candidate	TBD

Table 2. GN21-XA/X2 GDDR6 Recommended Memories

Memory Density	FBVDDQ	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Support GPU Min/Max
16Gb	2Ch512M16	1.35V 1.25V 1.1V	Samsung	K4ZAF328C-SC16	A-die	16 Gbps	2216	Full	Production candidate	PS or later
			Hynix	H56G4254D014	A-die	16 Gbps	2216	Full	Production candidate	PS or later
			Micron	MT61K032M28P9A-16C	C-die	16 Gbps	2216	Full	Production candidate	PS or later

Notes:

¹ Refer to the GN21/GA21/GA22 Product Specification for memory voltages and clocks.

² 1.17V is only available for the Samsung memory.

³ GN21-XA/GN21 with Base TDP between 35-50W will be single sourced with Samsung K4ZAF328C-SC16 for the foreseeable future until further notice from NVIDIA.

⁴ For GN21-XA/GN21, the maximum allowable memory case temperature is 95°C.

Samsung, K4ZAF328C-SC16	Strap2	Strap1	Strap0	RAMCFG
Hynix, H56G4254D014	L	M	M	0x0
Micron, MT61K032M28P9A-16C (GN21-X2/XA/X2)	L	M	L	0x0
Micron, MT61K032M28P9A-16C (GN20-P0-R)	H	H	H	0x1

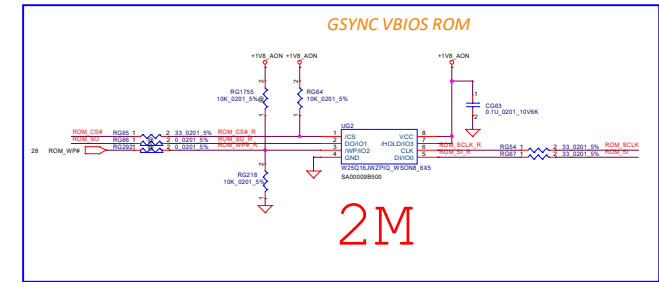
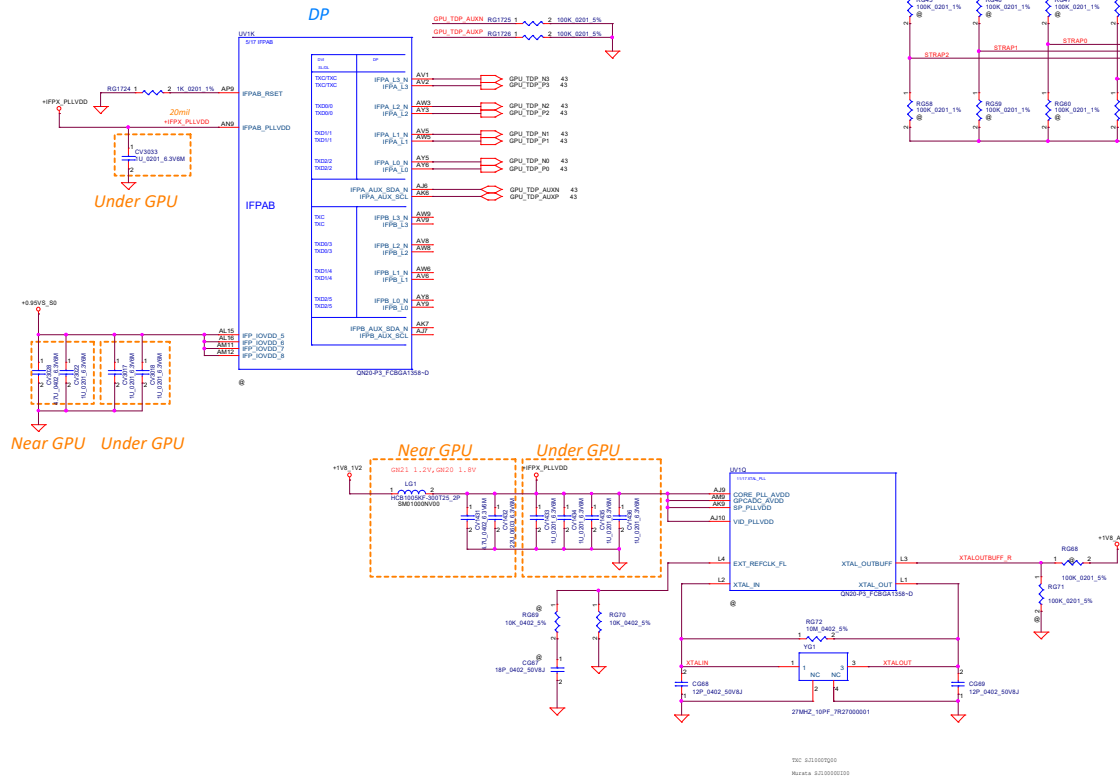
Samsung (GN21)	RG58 X78_GN21H06 100K_0201_1%	RG48 X78_GN21H06 200K_0201_1%	RG59 X78_GN21H06 100K_0201_1%	RG47 X78_GN21H06 100K_0201_1%
Hynix (GN21)	RG58 X78_GN21H06 100K_0201_1%	RG48 X78_GN21H06 200K_0201_1%	RG59 X78_GN21H06 100K_0201_1%	RG47 X78_GN21H06 100K_0201_1%
Micron (GN21)	RG58 X78_GN21H06 100K_0201_1%	RG48 X78_GN21H06 200K_0201_1%	RG59 X78_GN21H06 100K_0201_1%	RG47 X78_GN21H06 100K_0201_1%
Samsung (GN20-P0-R)	RG58 X78_GN20H06 100K_0201_1%	RG48 X78_GN20H06 200K_0201_1%	RG59 X78_GN20H06 100K_0201_1%	RG47 X78_GN20H06 100K_0201_1%
Hynix (GN20-P0-R)	RG58 X78_GN20H06 100K_0201_1%	RG48 X78_GN20H06 200K_0201_1%	RG59 X78_GN20H06 100K_0201_1%	RG47 X78_GN20H06 100K_0201_1%
Micron (GN20-P0-R)	RG48 X78_GN20H06 100K_0201_1%	RG46 X78_GN20H06 200K_0201_1%	RG47 X78_GN20H06 100K_0201_1%	

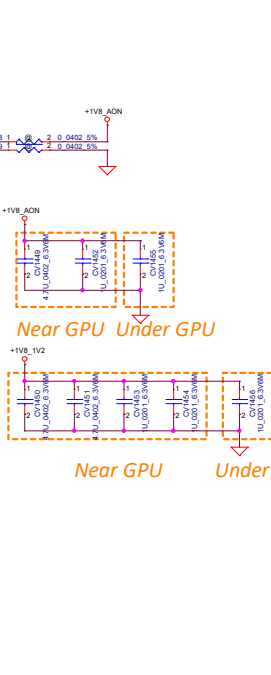
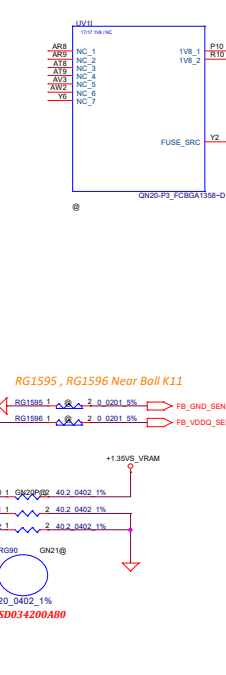
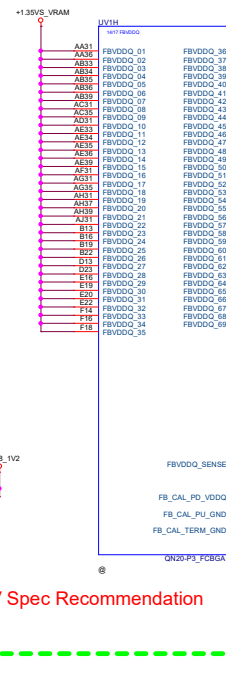
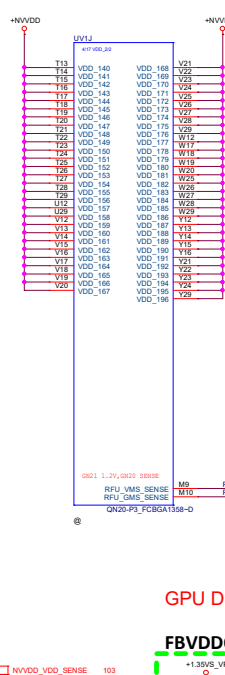
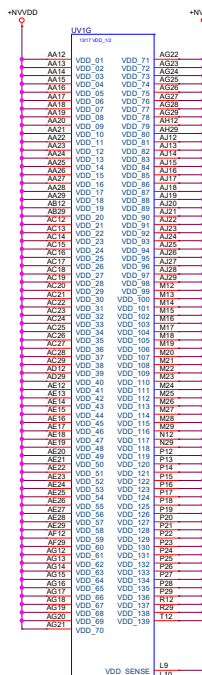
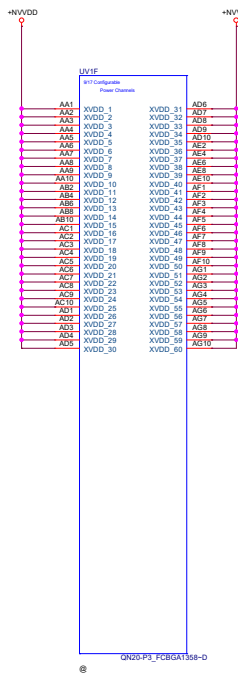
GN20 Middle 0.9V, GN21 Middle 0.6V

Table 11.4 FS_OVERT* Strap Enablement

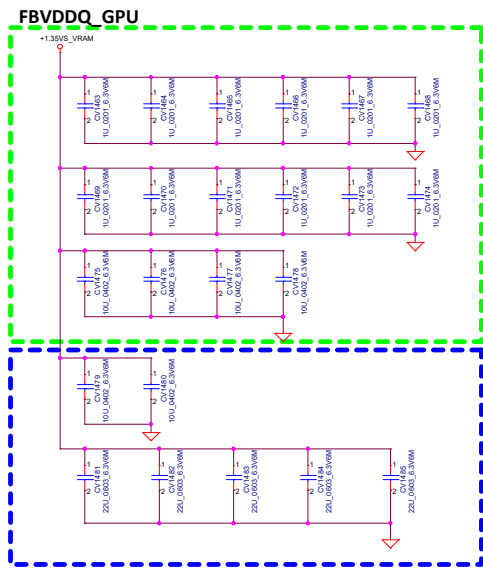
Strap Pins see Note			FS_OVERT*Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT*Function ENABLED
L	L	H	FS_OVERT*Function DISABLED (Relieved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.





GPU Decoupling - NV Spec Recommendation



Place under GPU

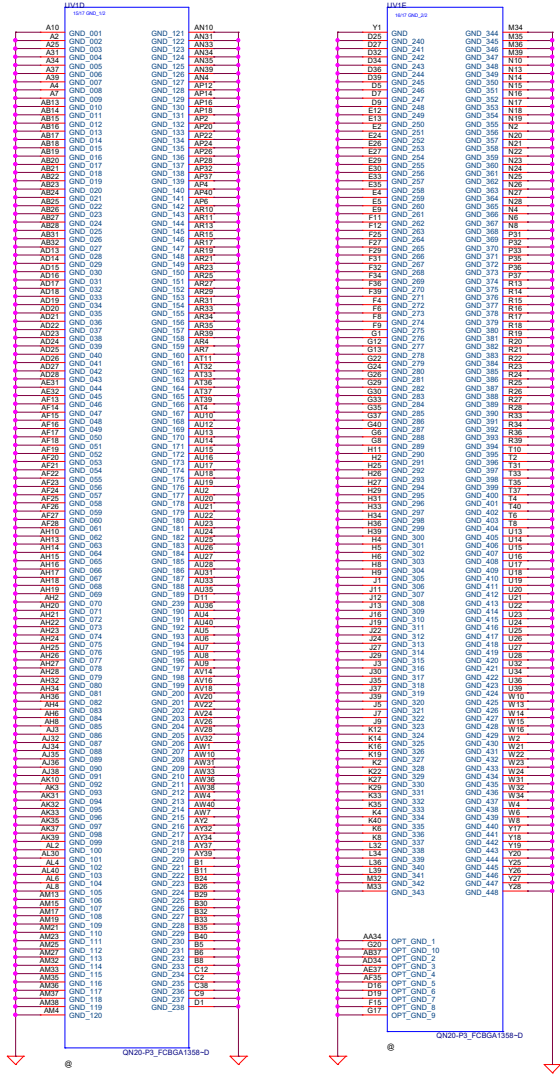
1UF_0402 X 12 pcs
10UF_0603 X 4 pcs

Place near GPU

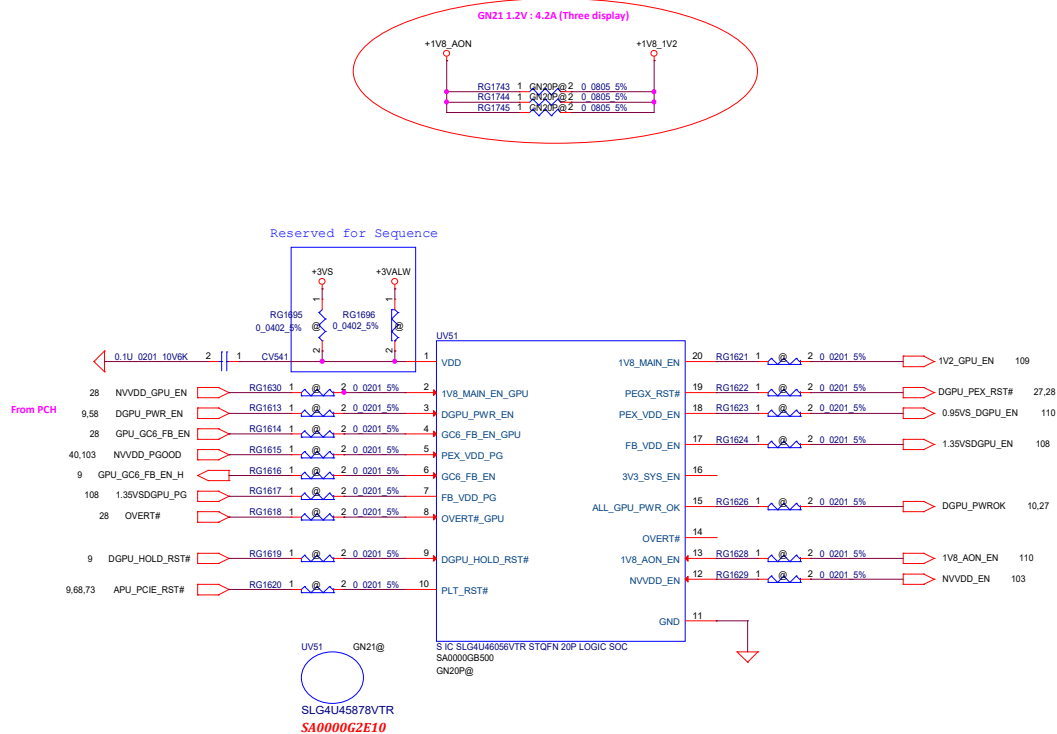
22UF_0603 X 5 pcs
10UF_0603 X 2 pcs

GPU	Capacitor Type	Footprint	Population		Location	
			GB5-128	GB5B-128		
FBVDD/Q Supply Rail						
GB5-128	1 μF	X6S	0402 or 0201W	12	12	Under GPU
GB5B-128	10 μF	X6S	0603	4	4	Under GPU
	10 μF	X6S	0603	2	2	Near GPU
	22 μF	X6S	0603W	5	5	Near GPU

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										Date		Wednesday, March 01, 2023		11:58:11	



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	1V2	1V8	NVDD	PEXVDD	VPP	FBVDD
GC6 3.0	ON	ON	OFF	OFF	ON	ON
GC-OFF	OFF	OFF	OFF	OFF	OFF	OFF

Figure 3. GB5C-128/GB5B-128/GB5-128 GPU Power-Up Sequence

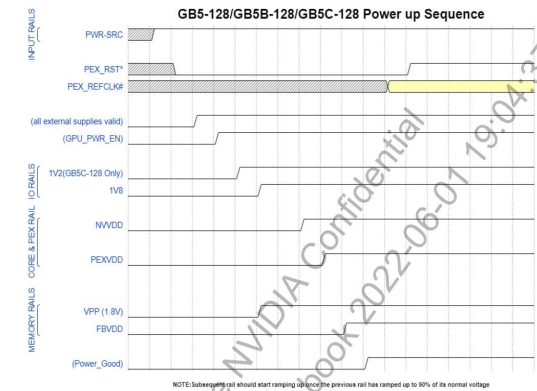


Figure 4. GB5C-128/GB5B-128/GB5-128 GPU Power Down Sequence

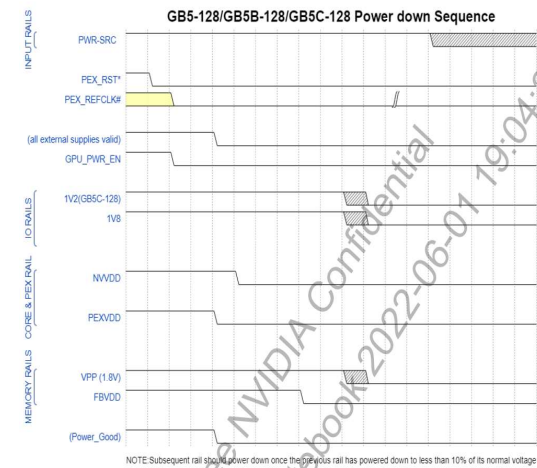
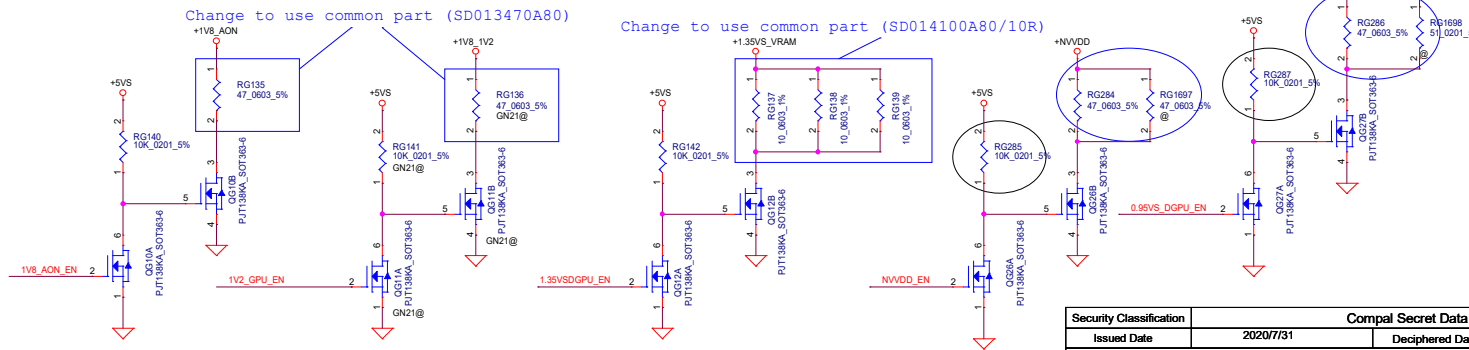
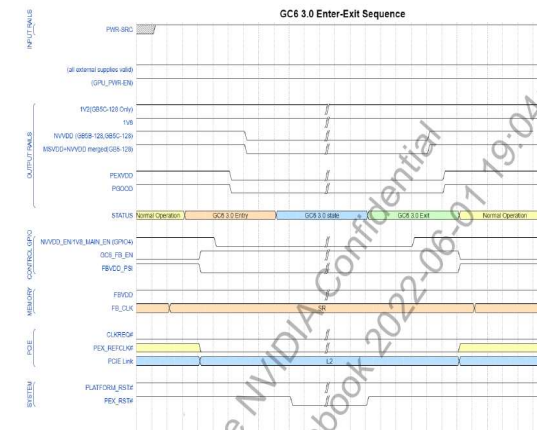


Figure 5. GB5C-128/GB5B-128/GB5-128 GPU GC6 3.0 Sequence



VRAM A

GA1XX GDDR6 CMD Mapping			
Lower 0..31		Upper 32..63	
DRAM1		DRAM2	
CH A-Byte 0..1		CH A-Byte 4..5	
CAD_A	CMD1	CMD33	
CAL_A	CMD13	CMD45	
CAL_B	CMD12	CMD35	
CAL_C	CMD24	CMD46	
CAL_D	CMD11	CMD36	
CAL_E	CMD15	CMD43	
CAL_F	CMD22	CMD49	
CAL_G	CMD23	CMD47	
CAL_H	CMD20	CMD34	
CAL_I	CMD2	CMD32	
CAL_J	CMD10	CMD37	
CAL_K	CMD14	CMD44	
CAL_L			
CAL_M			
CAL_N			
CAL_O			
CAL_P			
CAL_Q			
CAL_R			
CAL_S			
CAL_T			
CAL_U			
CAL_V			
CAL_W			
CAL_X			
CAL_Y			
CAL_Z			
RESET*	CMD3	CMD31	

CHB-Byte 2,3		CHB-Byte 6,7	
CAD_B	CMD5	CMD29	
CAL_B	CMD18	CMD52	
CAL_C	CMD7	CMD40	
CAL_D	CMD20	CMD39	
CAL_E	CMD8	CMD36	
CAL_F	CMD16	CMD42	
CAL_G	CMD21	CMD49	
CAL_H	CMD19	CMD51	
CAL_I	CMD6	CMD28	
CAL_J	CMD4	CMD30	
CAL_K	CMD9	CMD38	
CAL_L	CMD17	CMD41	
CAL_M			
CAL_N			
CAL_O			
CAL_P			
CAL_Q			
CAL_R			
CAL_S			
CAL_T			
CAL_U			
CAL_V			
CAL_W			
CAL_X			
CAL_Y			
CAL_Z			

RESET*	CMD3	CMD31	
--------	------	-------	--

RESET*	CMD3	CMD31	
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RESET*	CMD3	CMD31	
--------	------	-------	--

RESET*	CMD3	CMD31	
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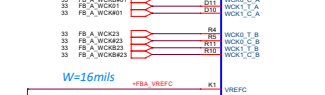
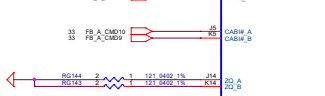
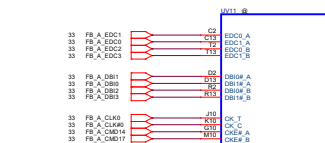
RESET*	CMD3	CMD31	
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RESET*	CMD3	CMD31	
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RESET*	CMD3	CMD31	
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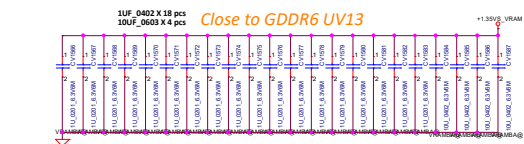
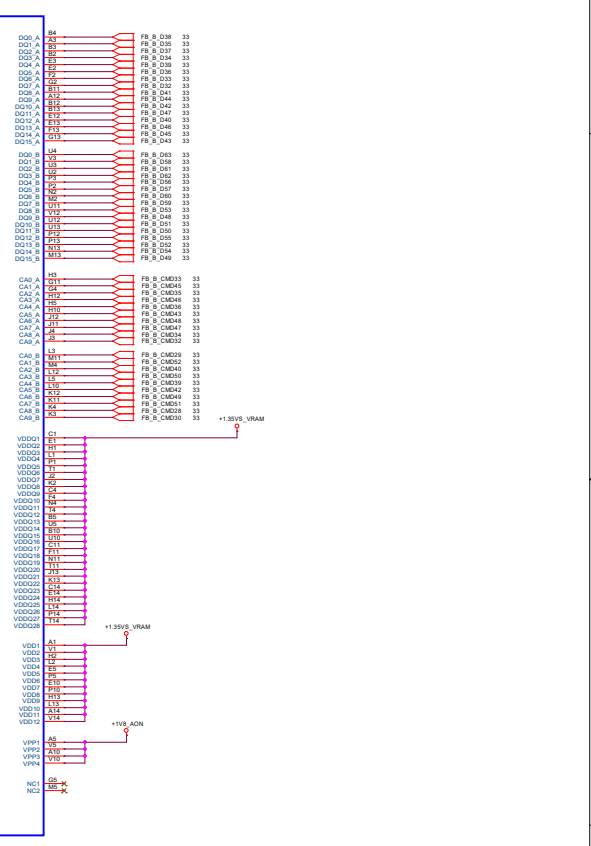
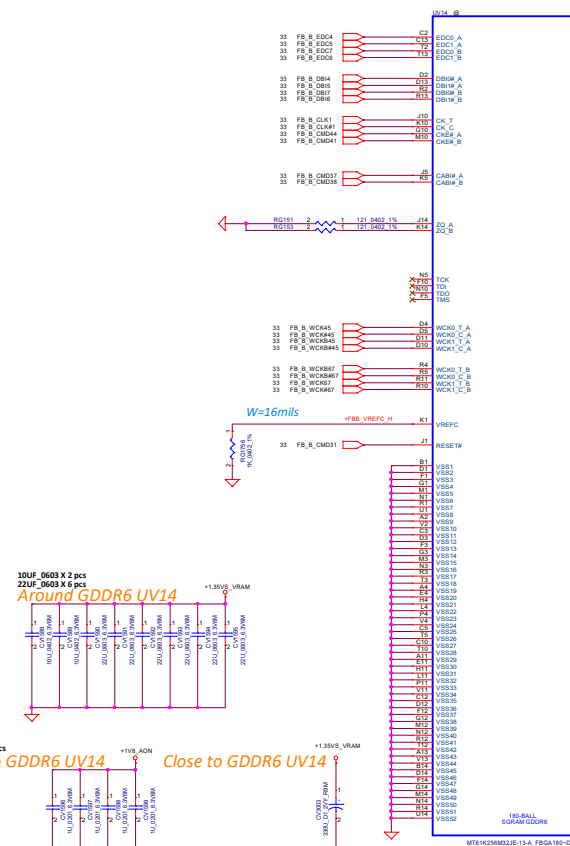
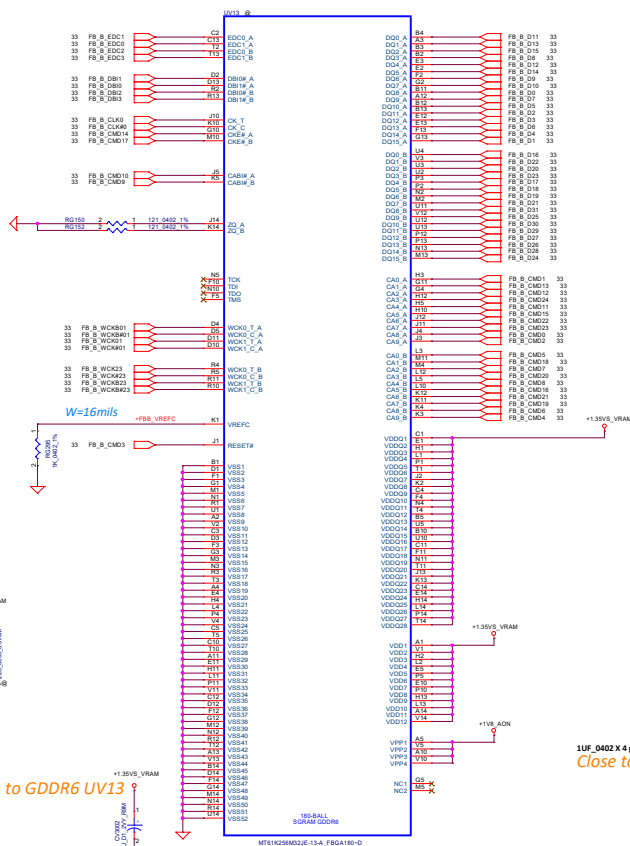
RESET*	CMD3	CMD31	
--------	------	-------	--

RESET*	CMD3	CMD31	
--------	------	-------	--



VRAM B

GA1XX GDDR6 CMD Mapping		
Lower 0.31 DRAM1 CHA-Byte 0,1		Upper 0.31 DRAM1 CHA-Byte 4,5
CA0_A	CM01	CM033
CA1_A	CM013	CM045
CA2_A	CM012	CM035
CA3_A	CM024	CM046
CA4_A	CM011	CM036
CA5_A	CM015	CM043
CA6_A	CM022	CM048
CA7_A	CM023	CM047
CA8_A	CM020	CM032
CA9_A	CM02	CM037
CAB_A	CM010	CM034
CAC_A	CM014	CM044
CA0_B	CM05	CM029
CA1_B	CM018	CM052
CA2_B	CM07	CM040
CA3_B	CM030	CM050
CA4_B	CM08	CM039
CA5_B	CM016	CM042
CA6_B	CM021	CM049
CA7_B	CM09	CM051
CA8_B	CM04	CM038
CA9_B	CM06	CM031
CAB_B	CM03	CM041
CAC_B	CM031	CM043



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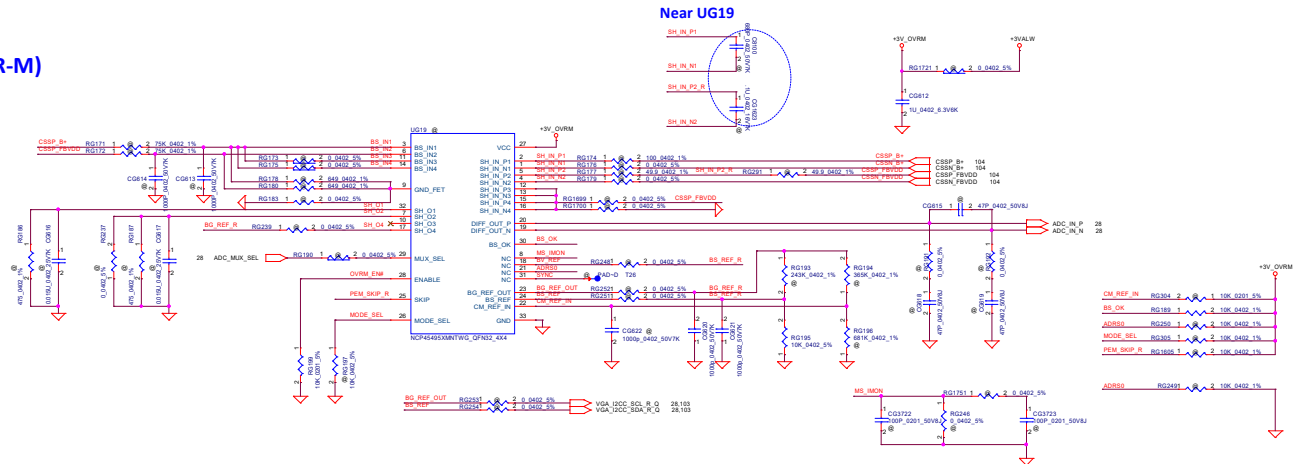
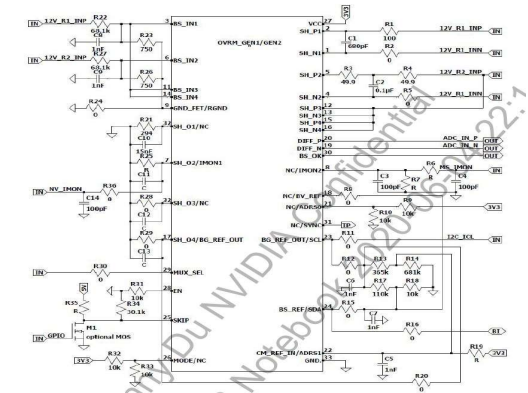
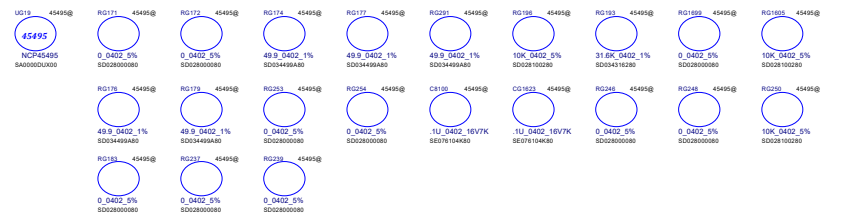


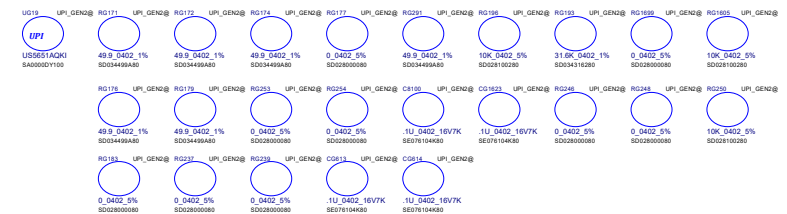
Figure 3.5 OVR-M GEN1 and GEN2 Co-Design



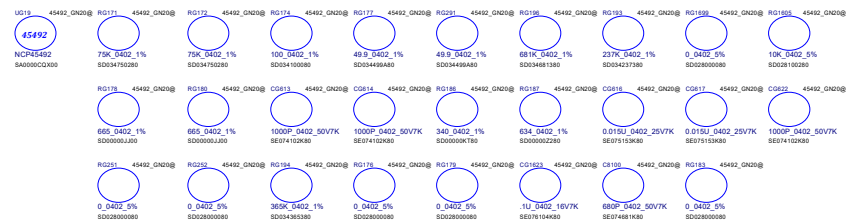
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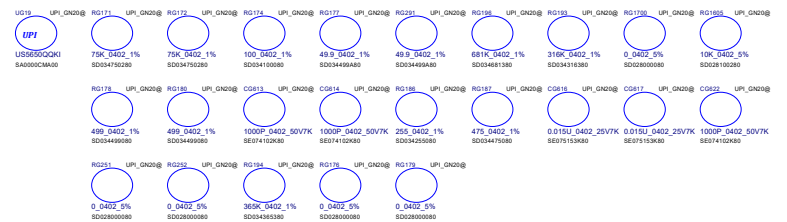
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OVR-M Gen1 Onsemi (GN20)



OVR-M Gen1 UPI (GN20)

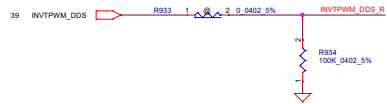


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DISPLAY OFF

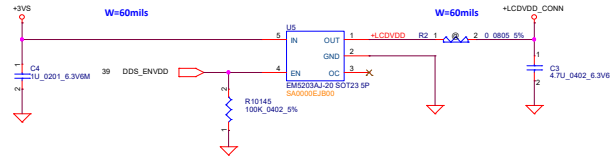


PWM

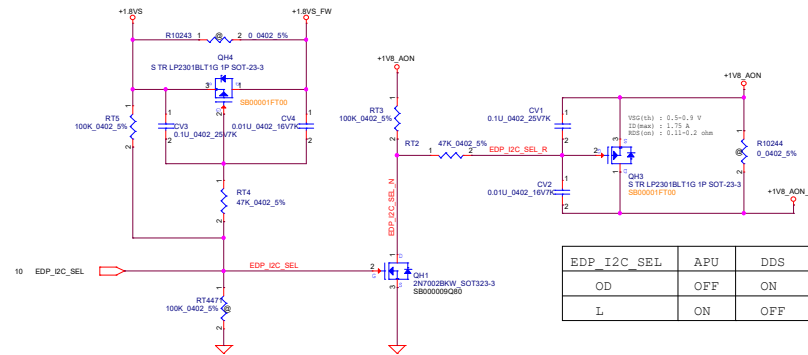


HOT PLUG DETECT

LCD POWER SWITCH

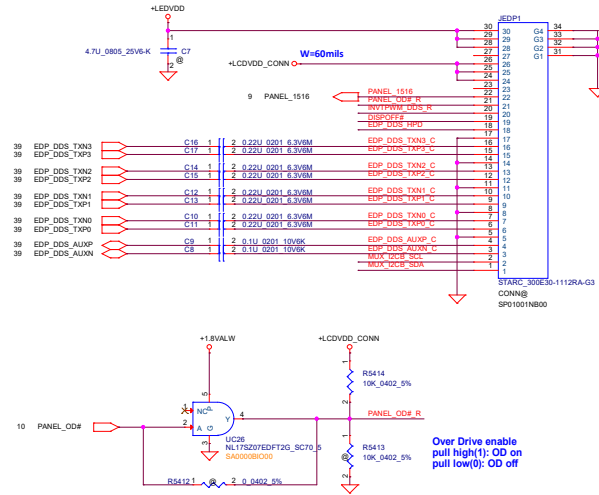


Panel FW update



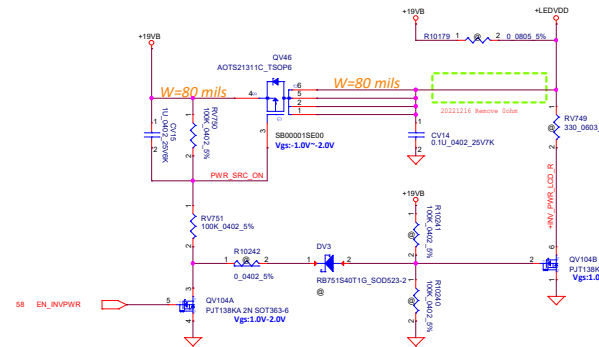
EDP I2C_SEL	APU	DDS
OD	OFF	ON
L	ON	OFF

eDP CONNECTOR

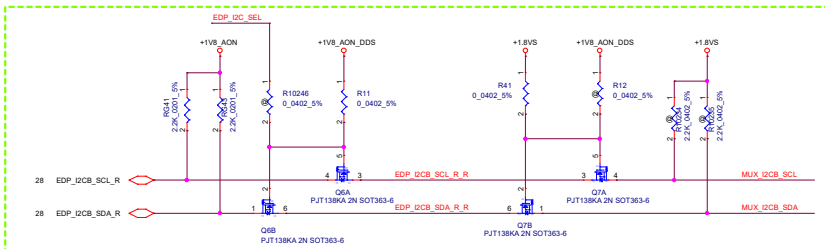


From CPU

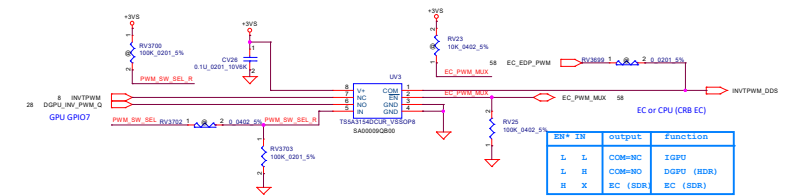
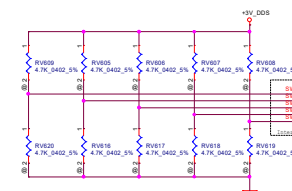
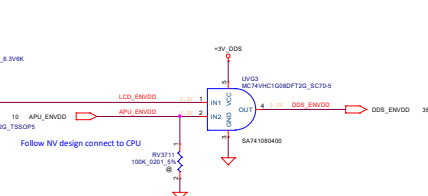
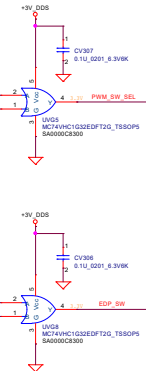
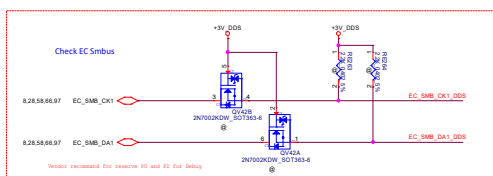
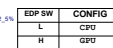
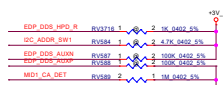
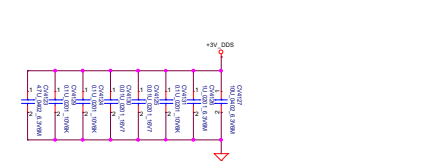
PANEL 20V DISCHARGE



From GPU



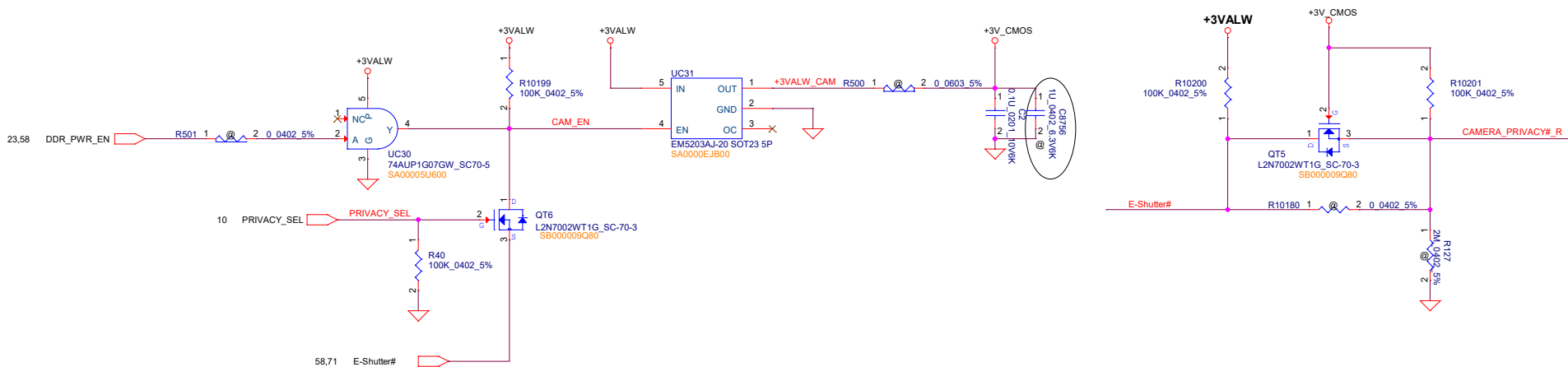
Check AMD MS GC6 leakage



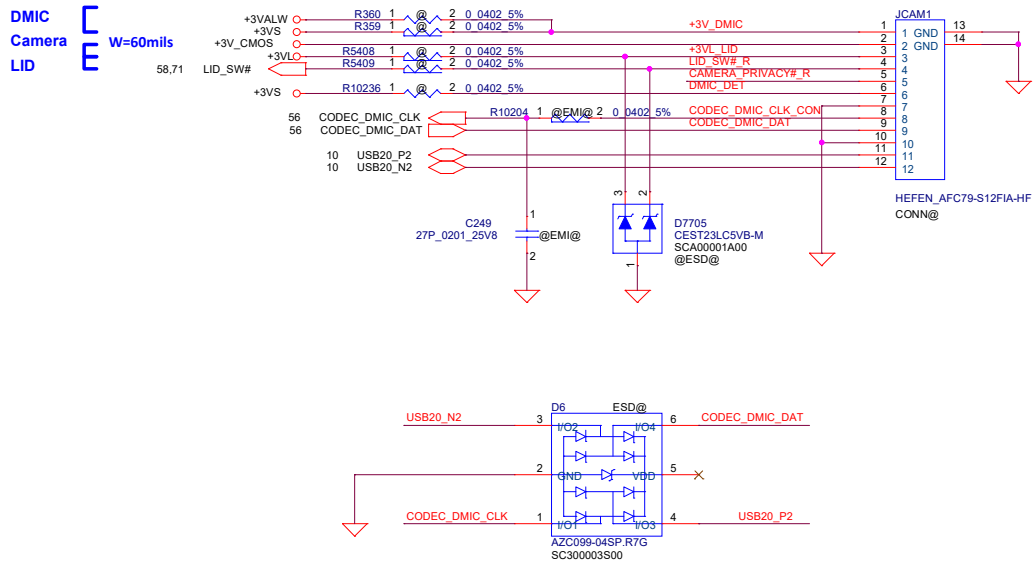
EN* IN	output	function
L L	COM=NC	IGPU
L H	COM=NO	DGPU (HDR)
H X	EC (SDR)	EC (SDR)

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CAMERA POWER CIRCUIT



	PRIVACY_SEL (From BIOS)	E-Shutter#	CAMERA_PRIVACY#	Camera Power
For Privacy	0	0	0	ON
		1	1	ON
For non Privacy	1	0	(don't care)	OFF
		1	(don't care)	ON



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I2C EC Address
USBC0 : 01000000
USBC1 : 01001000

EC

APU, ROM, Retimer

APU, ROM, Retimer

I2C Address : 0x50

512Kbit

Table 8-2. Decoding of ADCIN1 and ADCIN2 Pins			
DIV = R _{DOWN} / (R _{UP} + R _{DOWN}) ⁽¹⁾		Without using R _{UP} or R _{DOWN}	
MIN	Target	MAX	ADCINx decoded value
0	0.0114	0.0228	tie to GND
0.0228	0.0475	0.0722	N/A
0.0722	0.1074	0.1425	N/A
0.1425	0.1899	0.2372	N/A
0.2372	0.3022	0.3671	N/A
0.3672	0.5368	0.7064	tie to LDO_V5
0.7065	0.8062	0.9060	N/A
DIV = R _{DOWN} / (R _{UP} + R _{DOWN}) ⁽¹⁾		Without using R _{UP} or R _{DOWN}	
MIN	Target	MAX	ADCINx decoded value
0.9061	0.9530	1.0	tie to LDO_V3V3

USB2.0

From PS8812

PS8812

USB2.0

LT4 Y580 EMI@

10 USB20_N0 4 3 USB20_N0_R

10 USB20_P0 1 2 USB20_P0_R

SM070005U00
DLM0NSN900HY2D_4P

Signal	PS8818 Pin
44 USB0_ATX_C_DRX_P1	PS8818 Pin 1
44 USB0_ATX_C_DRX_N1	
44 USB0_ARB_C_DTX_P1	PS8818 Pin 2
44 USB0_ARB_C_DTX_N1	
44 USB0_ATX_C_DRX_P2	PS8818 Pin 3
44 USB0_ATX_C_DRX_N2	
44 USB0_ARB_C_DTX_P2	PS8818 Pin 4
44 USB0_ARB_C_DTX_N2	

[illegible]

DT35

USBC0_SBU1_CONN 1 2

PESD24VF1BL SOD882-2
Y580_ESD@ SC40000I500

DT37

USBC0_CC1_CONN 1 2

PESD24VF1BL SOD882-2
Y580_ESD@ SC40000I500

DT36

USBC0_SBU2_CONN 1 2

PESD24VF1BL SOD882-2
Y580_ESD@ SC40000I500

DT38

USBC0_CC2_CONN 1 2

PESD24VF1BL SOD882-2
Y580_ESD@ SC40000I500

DT32

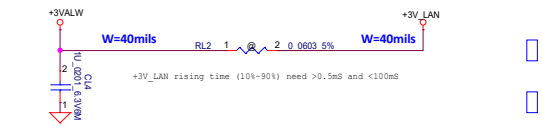
Y580_ESD@

USB20_N0_R 3 6

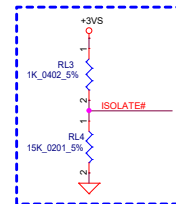
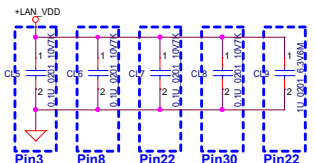
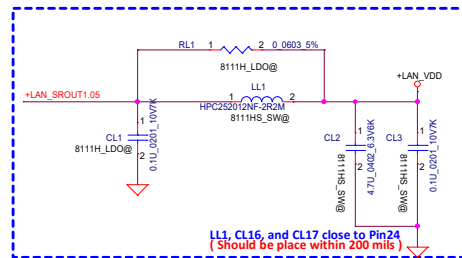
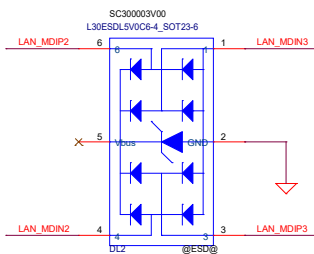
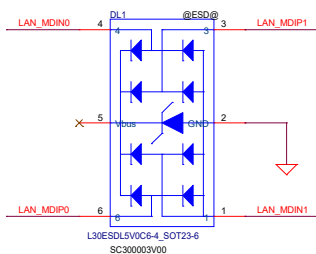
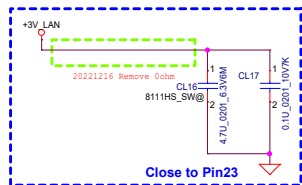
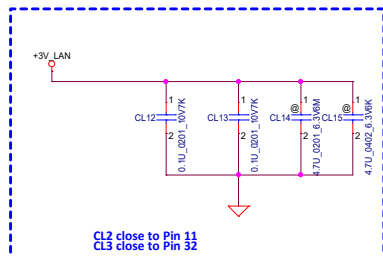
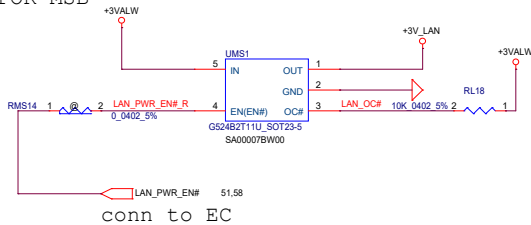
USB20_P0_R 1 4

AZC399-04S.R7G_SOT23-6
SC300005Y00

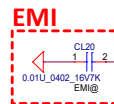
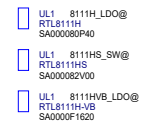
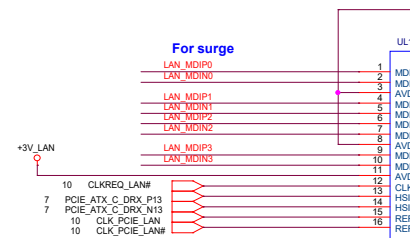
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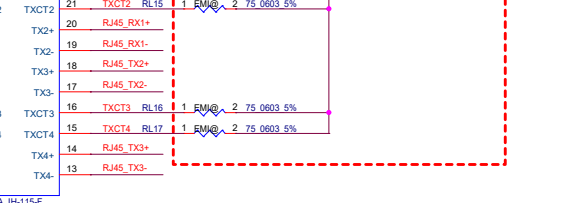
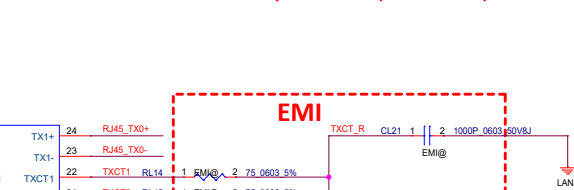
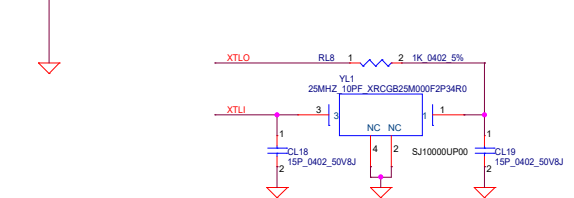
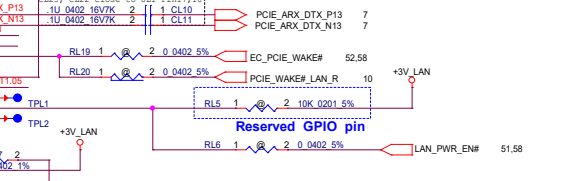
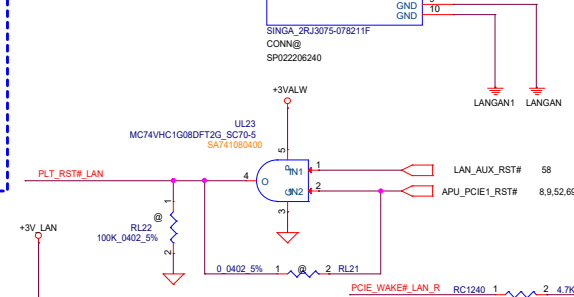
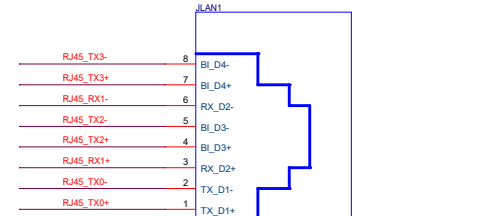
FOR MSB



For surge

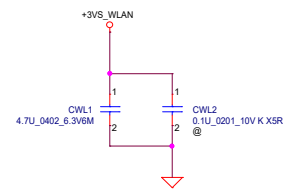
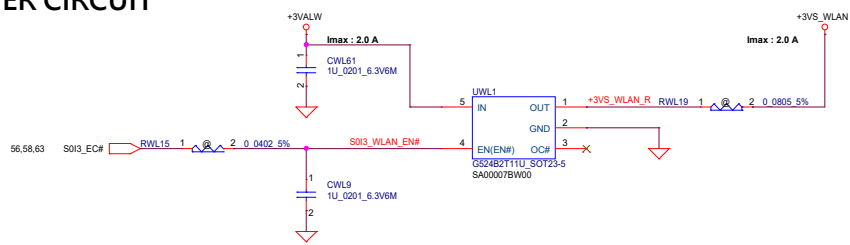


RJ-45 CONN.

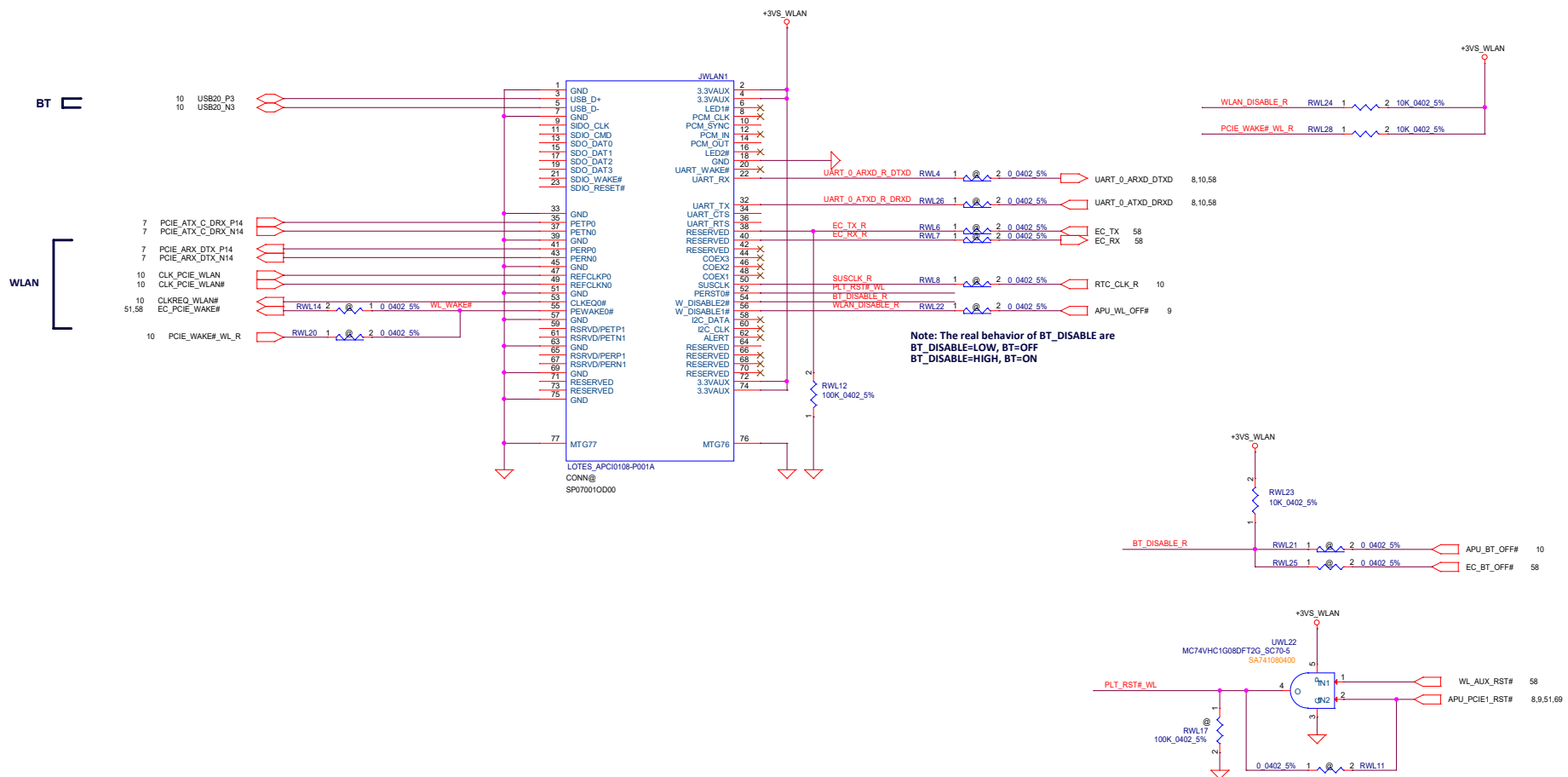


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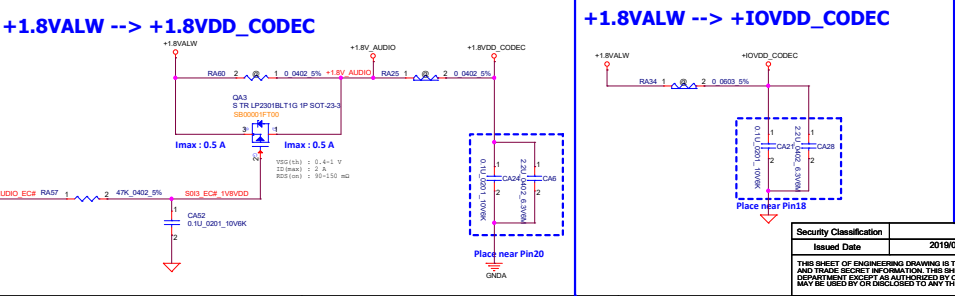
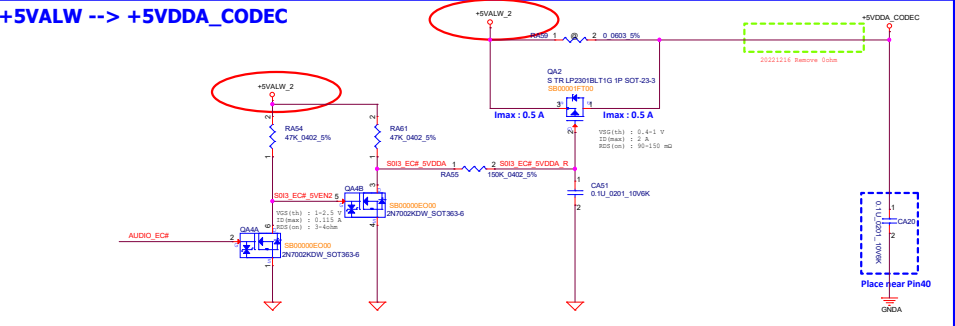
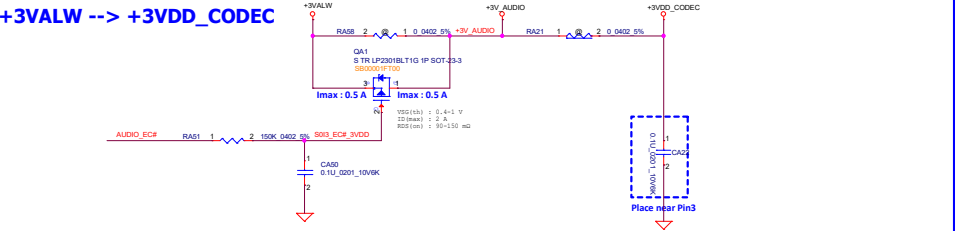
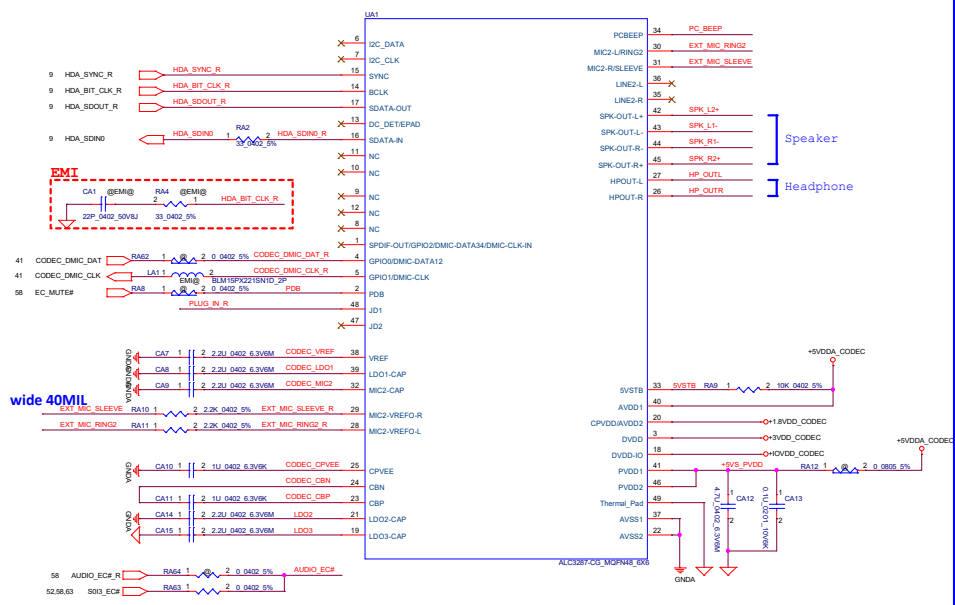
WLAN POWER CIRCUIT



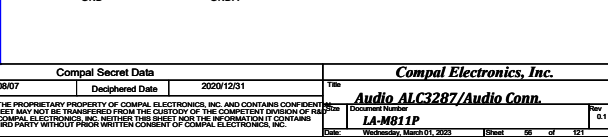
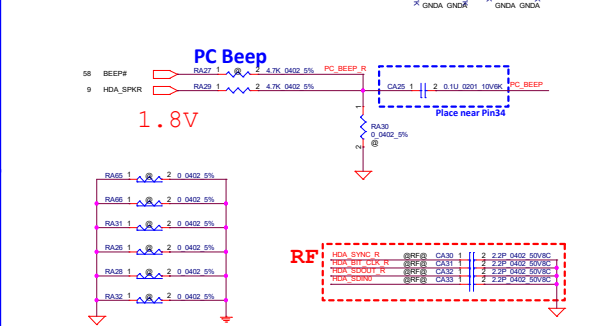
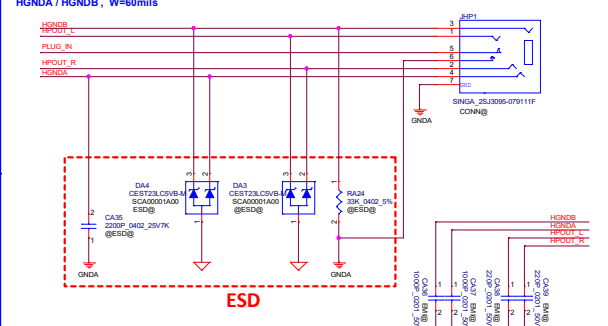
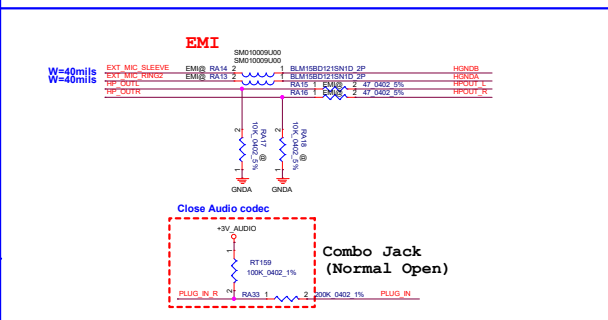
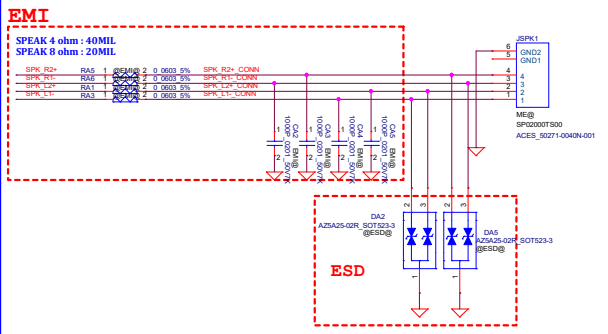
NGFF - WLAN / BT CONNECTOR (KEY-E)



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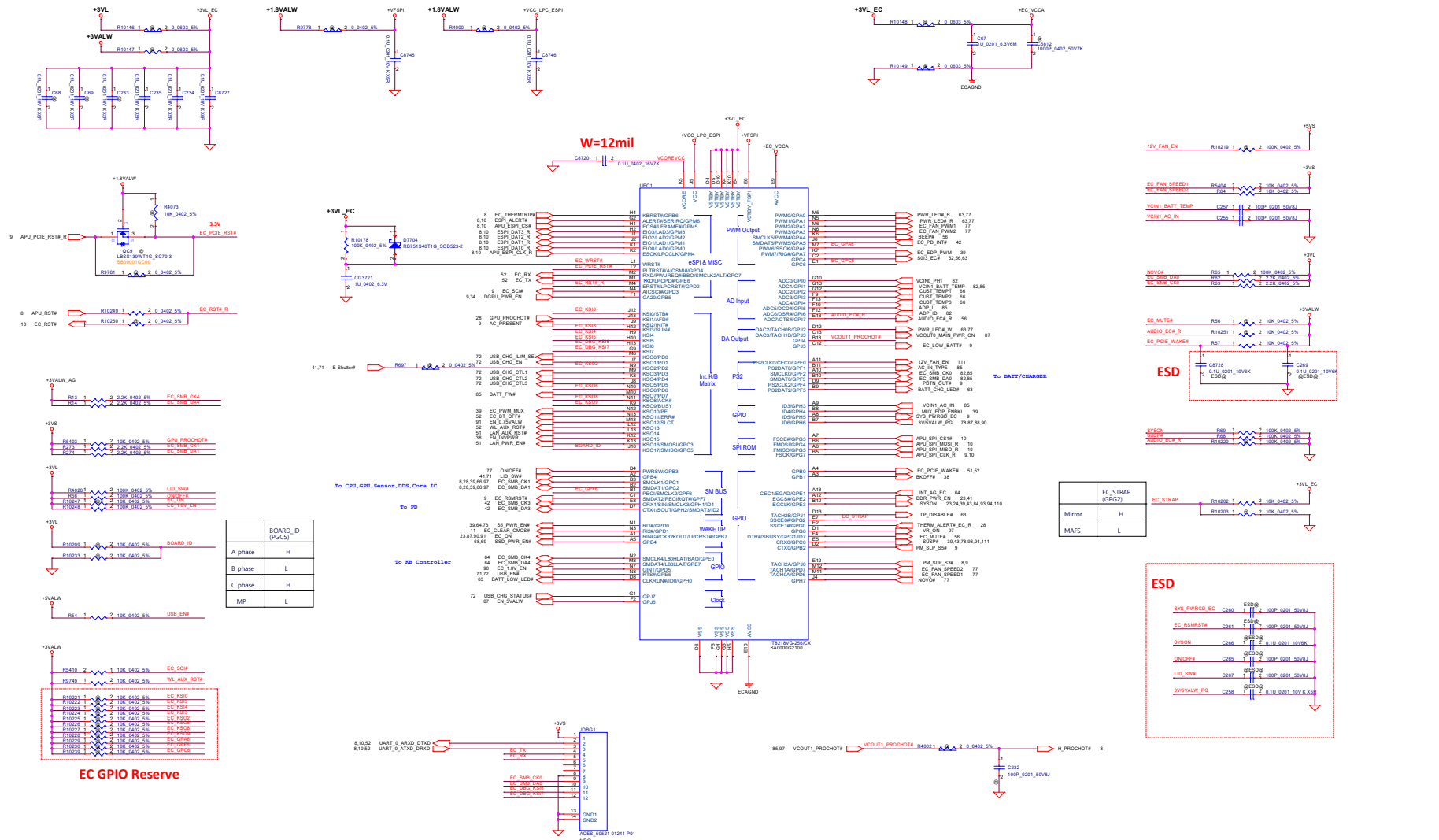


Speaker



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2019/08/07	2020/12/31	Audio ALC3287/Audio Conn.
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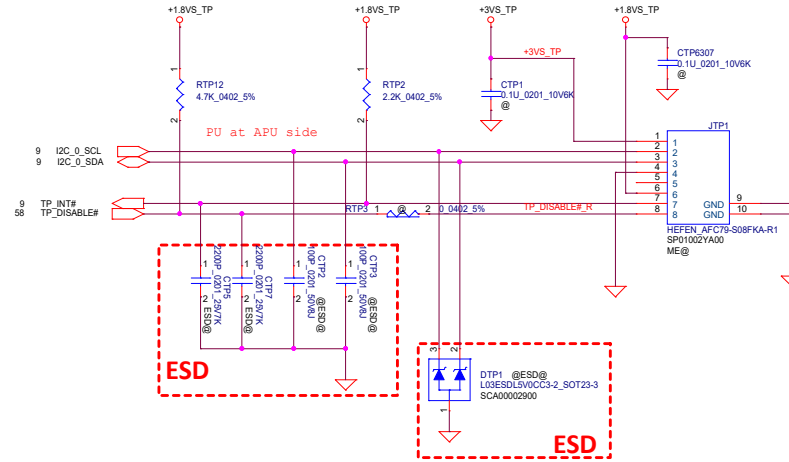
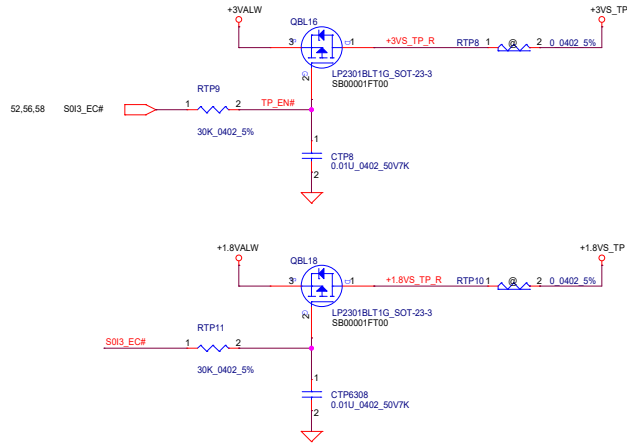
Embedded Controller



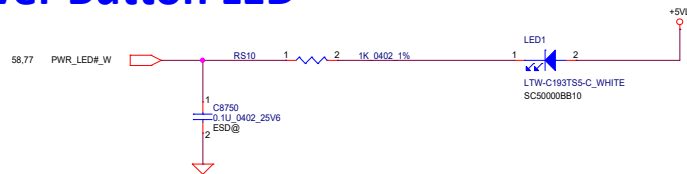
Main Func = EC

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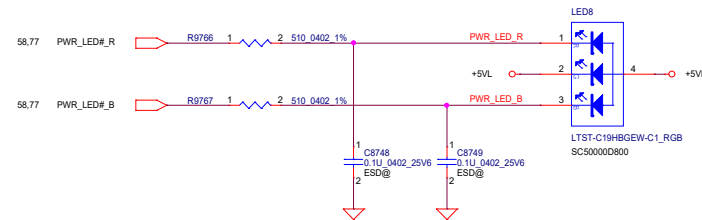
Touch Pad



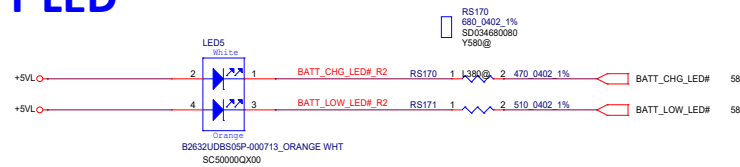
Power Button LED



RGB LED

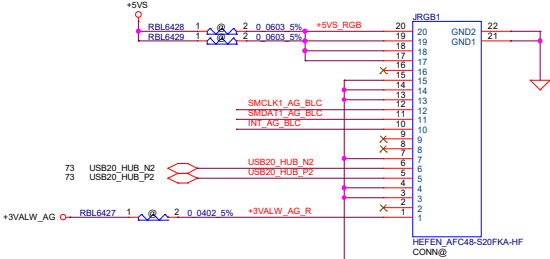


BATT LED

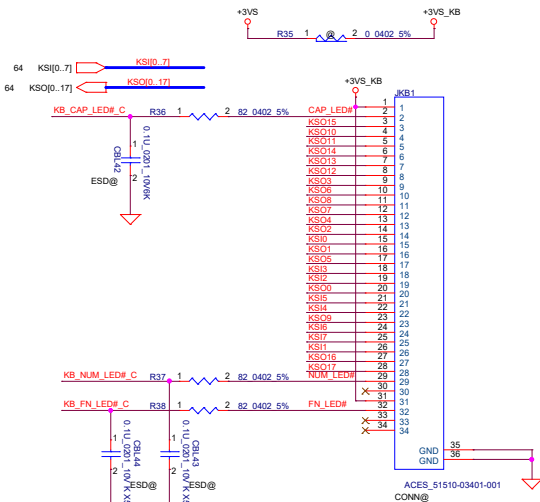


Title		LED/ TP/ USB IO	
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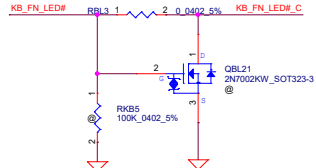
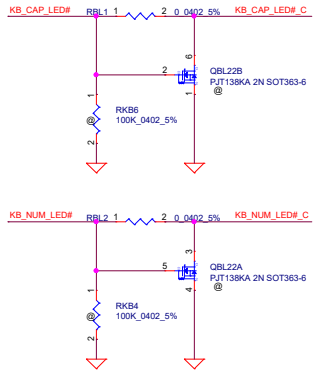
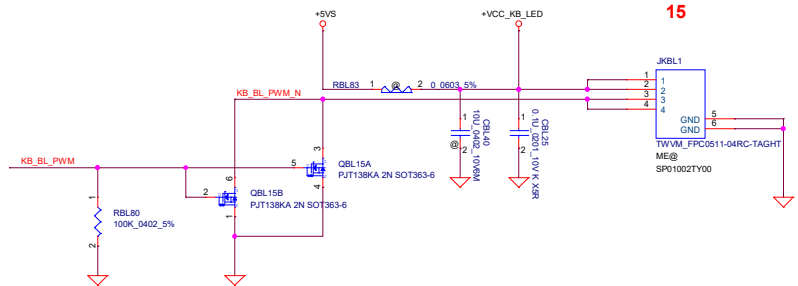
Keyboard RGB Backlight



Keyboard

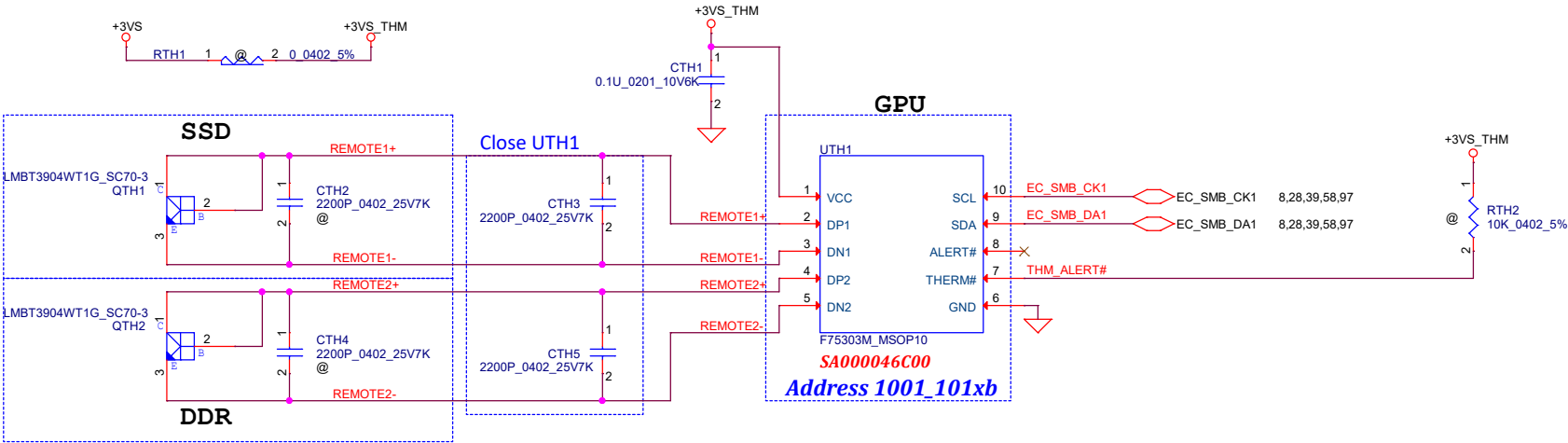


Keyboard Backlight



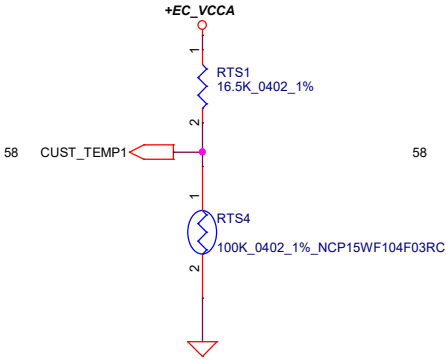
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Size	Document Number		
	CustomLA-MB11P		
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THERMAL SENSOR For Smart Performance

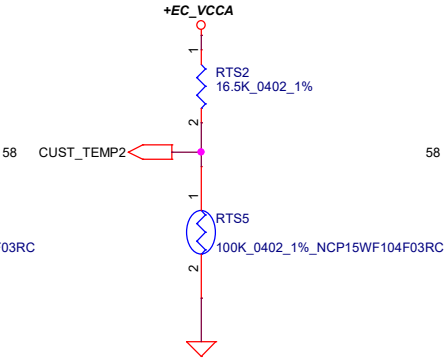


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Trace length:<8"

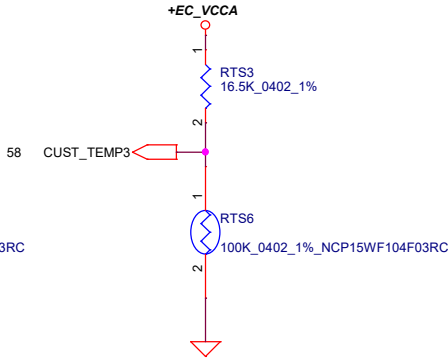
Left Fin



VCORE

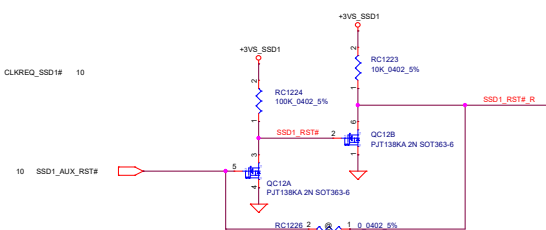
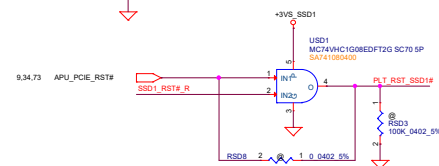
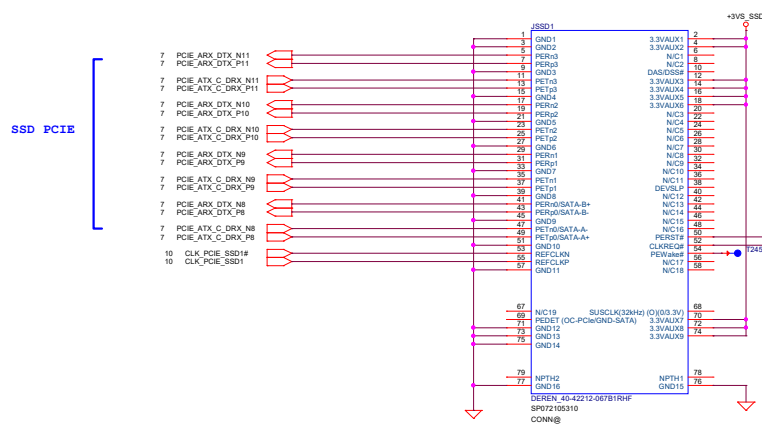
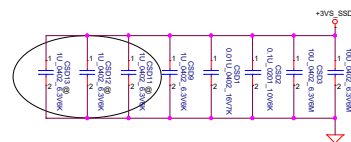
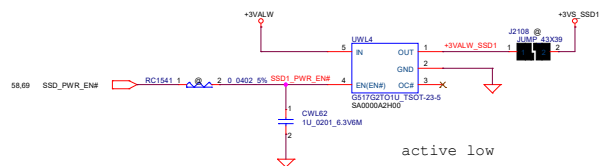


Right Fin



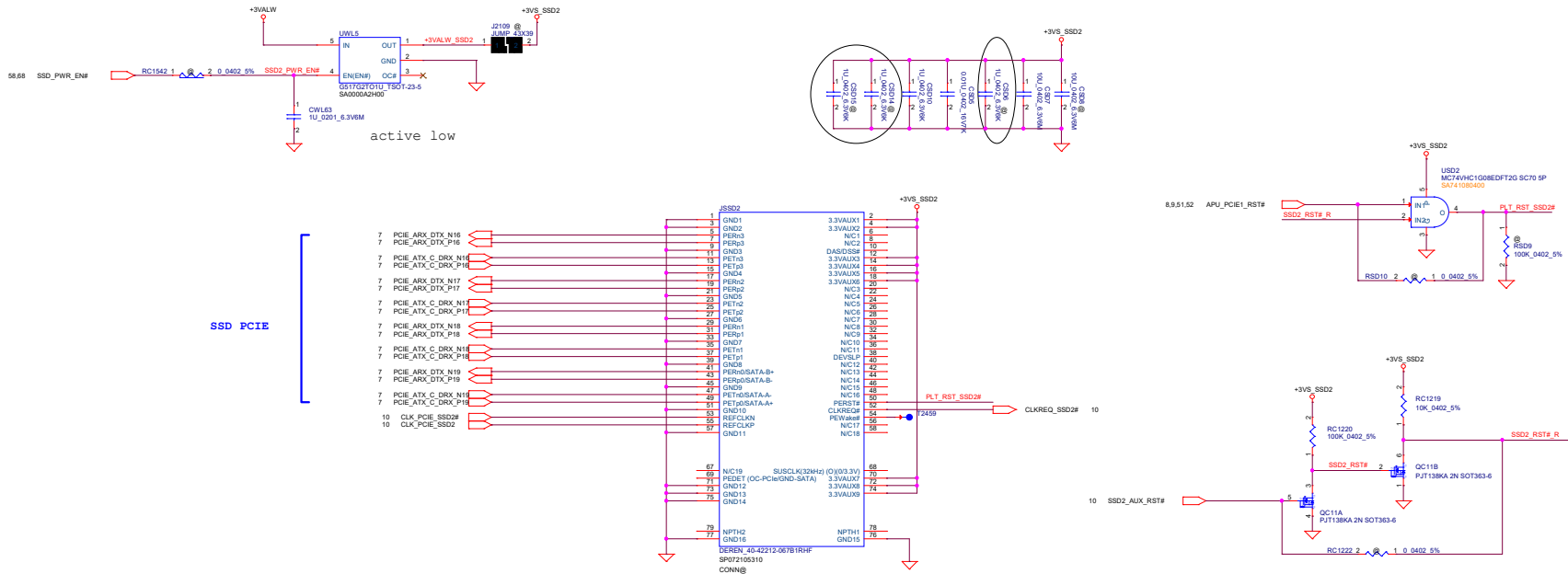
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SSD_2280 (TYPE M)

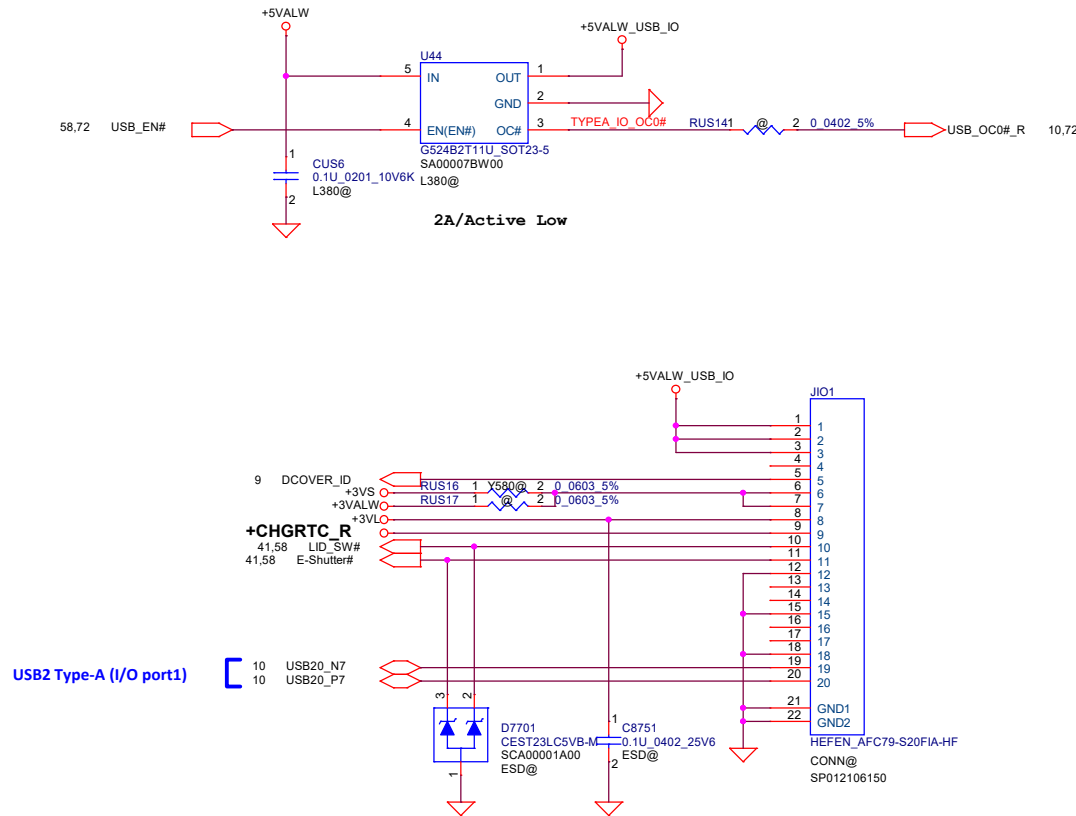


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			Doc No	LA-M811P
			Date	Wednesday, March 31, 2022
			Sheet	68 of 121

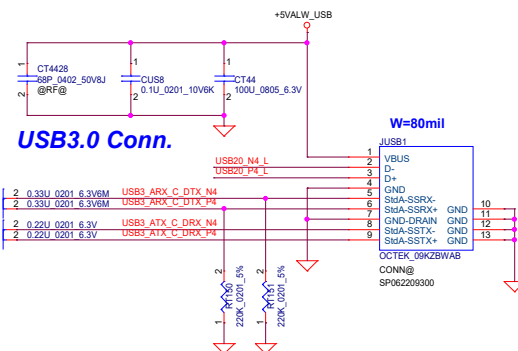
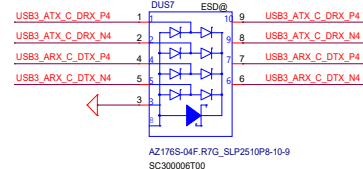
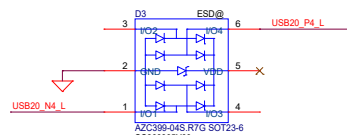
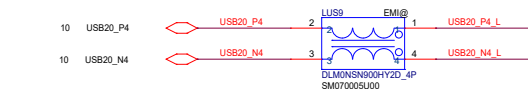
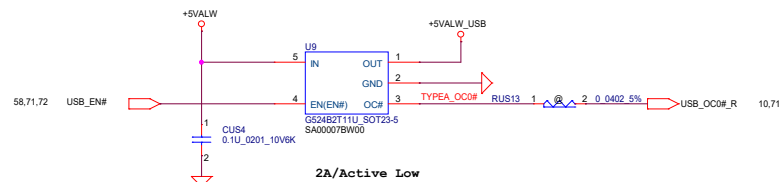
SSD_2242 (TYPE M)



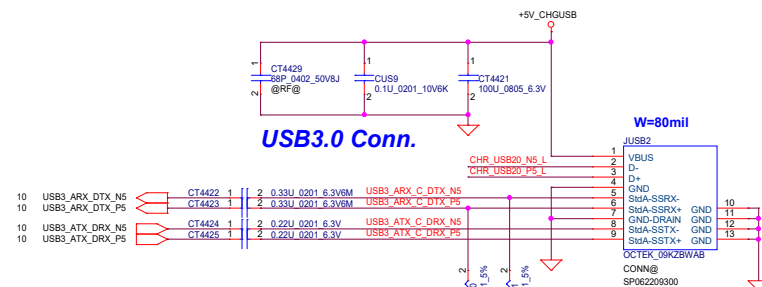
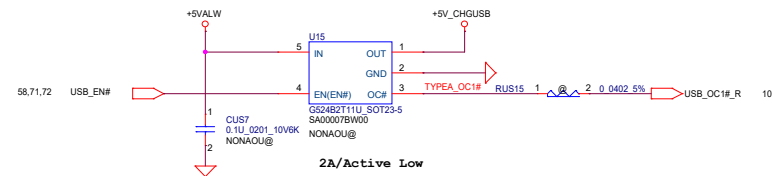
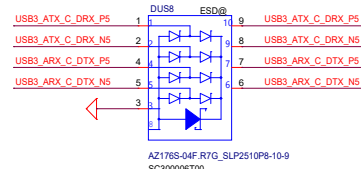
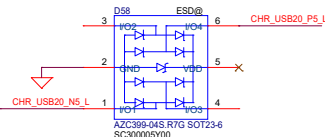
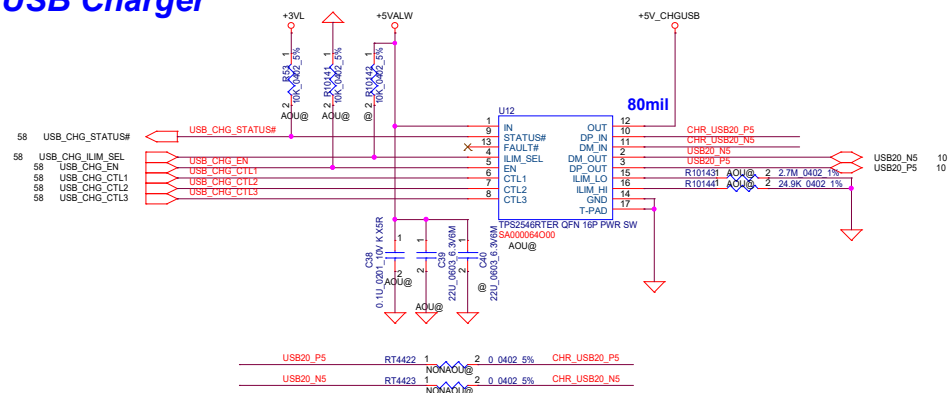
IO connector



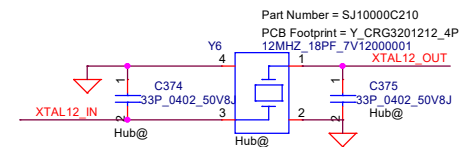
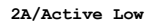
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USB Charger

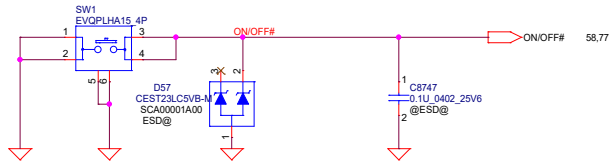


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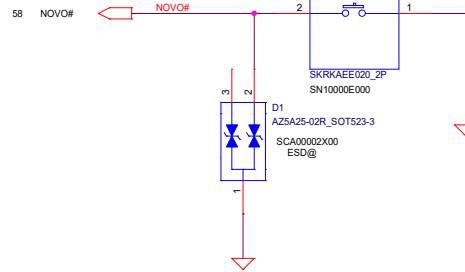


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				Size Document Number Rev Custom LA-M811P 0.1		
				Date: Wednesday, March 01, 2023 Sheet 73 of 121		

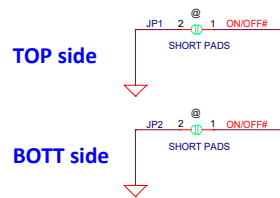
Power Button



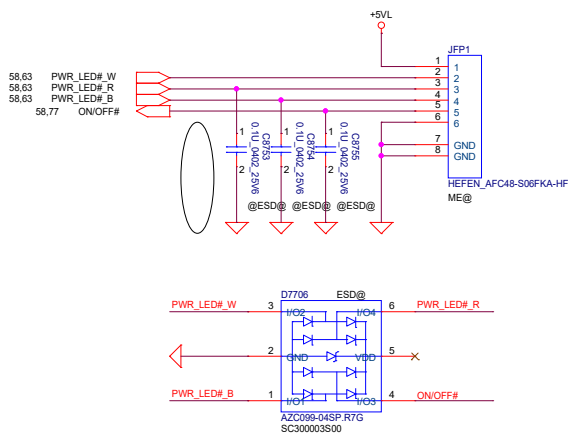
NOVO Button



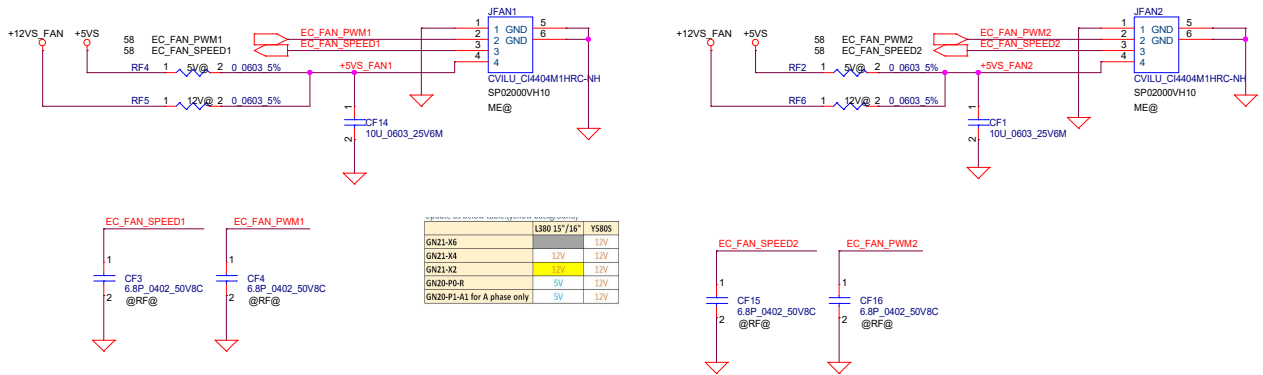
ON/OFF# SHORT PAD



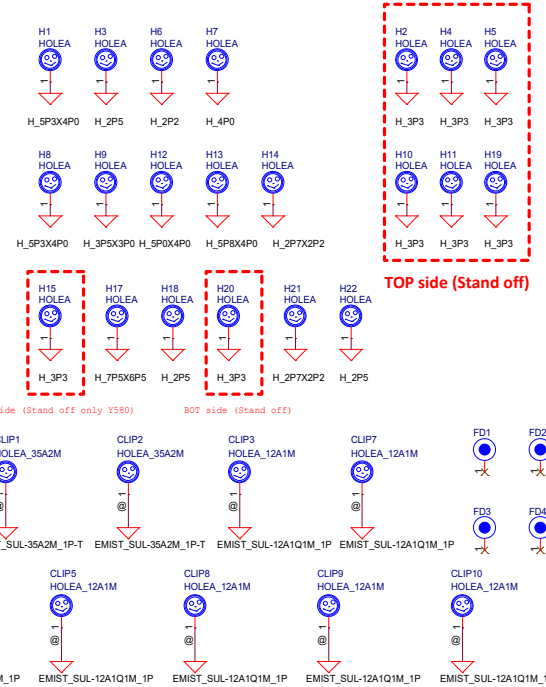
For Y580 Power button



FAN



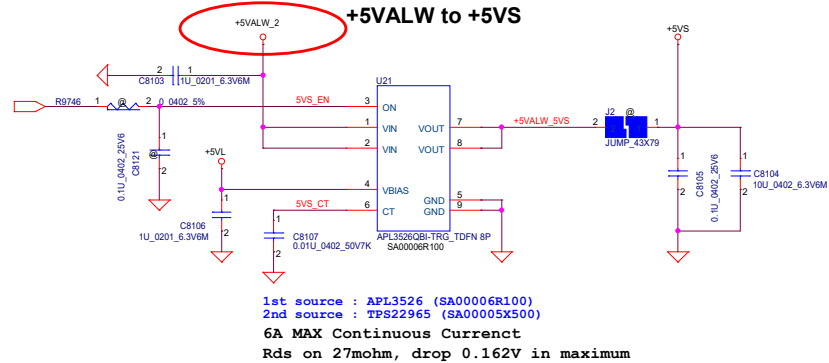
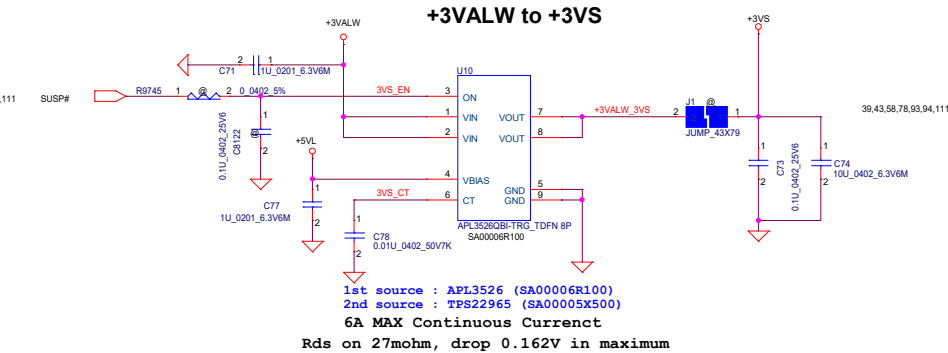
SCREW



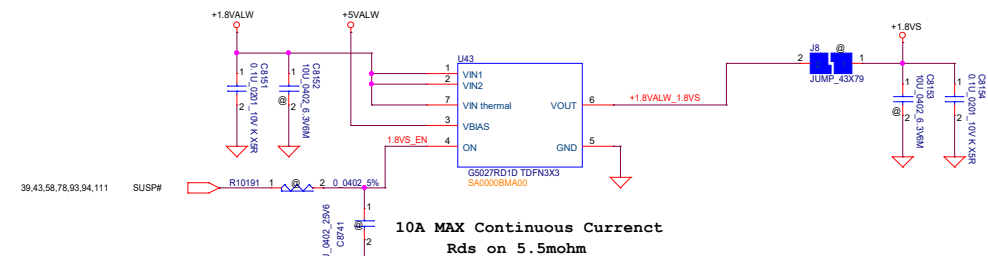
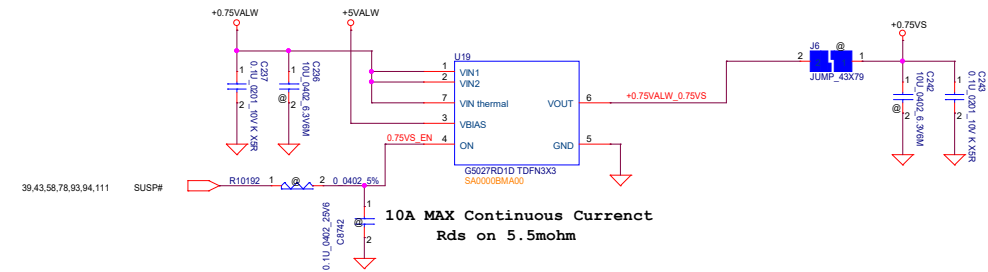
CLIP

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				LA-M811P	0.1
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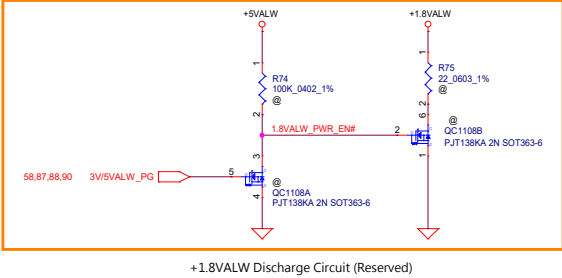
DC to DC



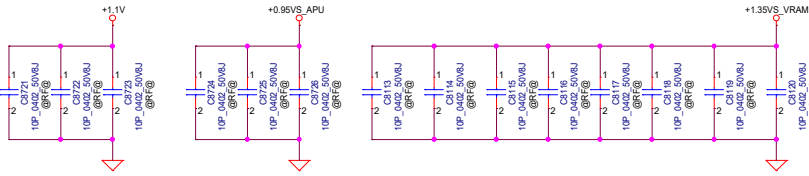
+1.8VALW to +1.8VS / +0.75VALW to +0.75VS

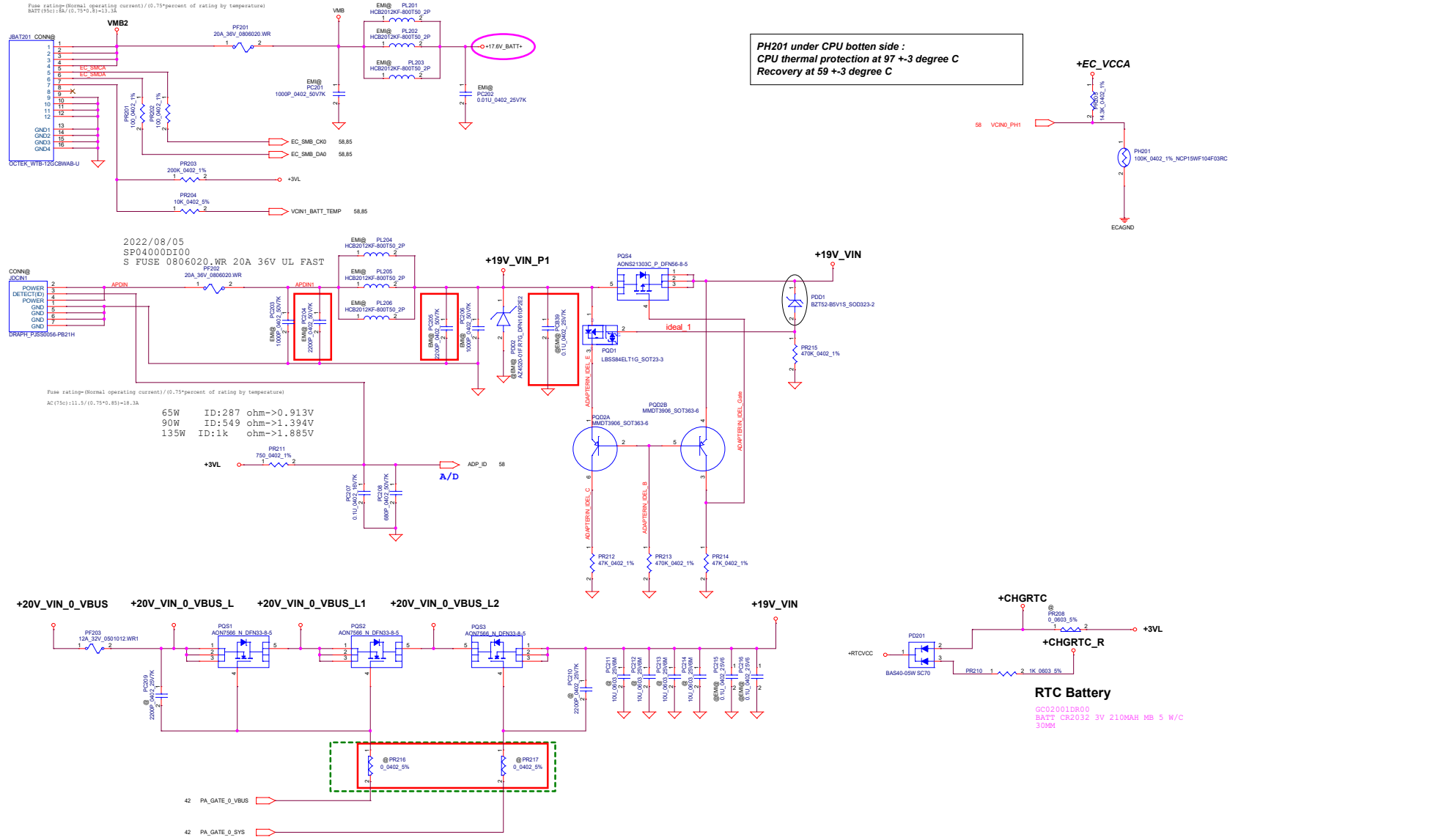


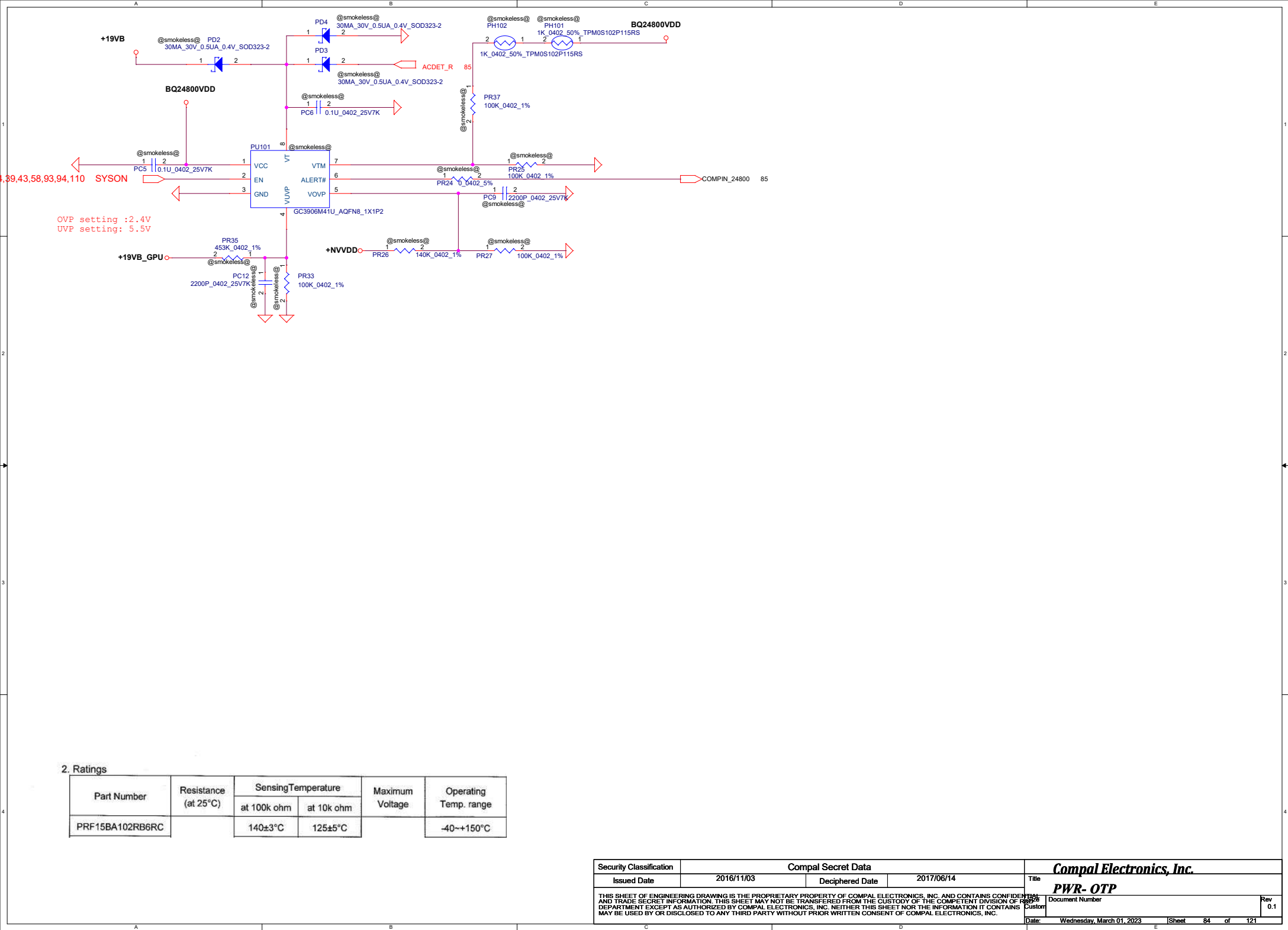
DISCHARGE CIRCUIT



RF



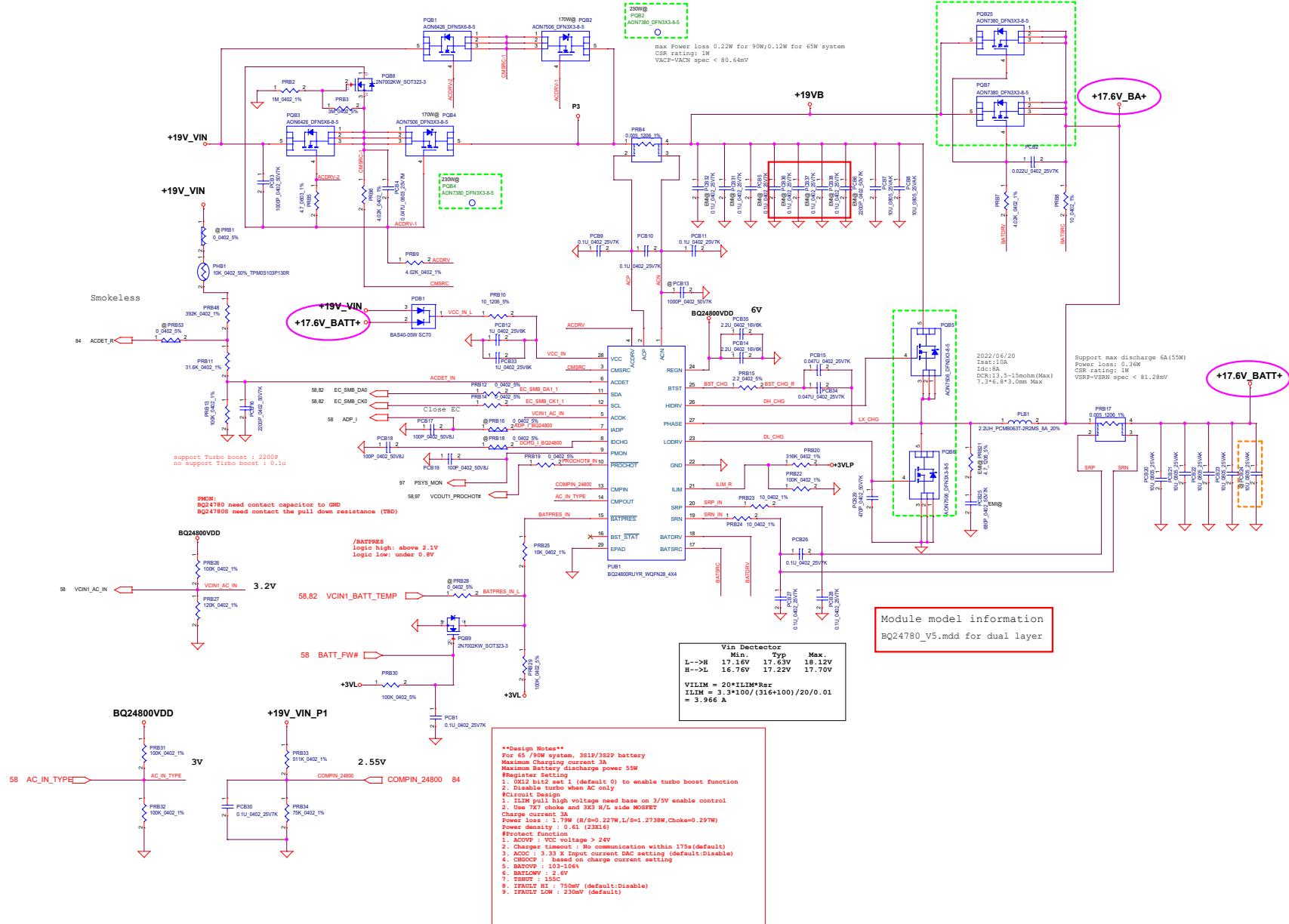




2. Ratings

Part Number	Resistance (at 25°C)	SensingTemperature		Maximum Voltage	Operating Temp. range
		at 100k ohm	at 10k ohm		
PRF15BA102RB6RC		140±3°C	125±5°C		-40~+150°C

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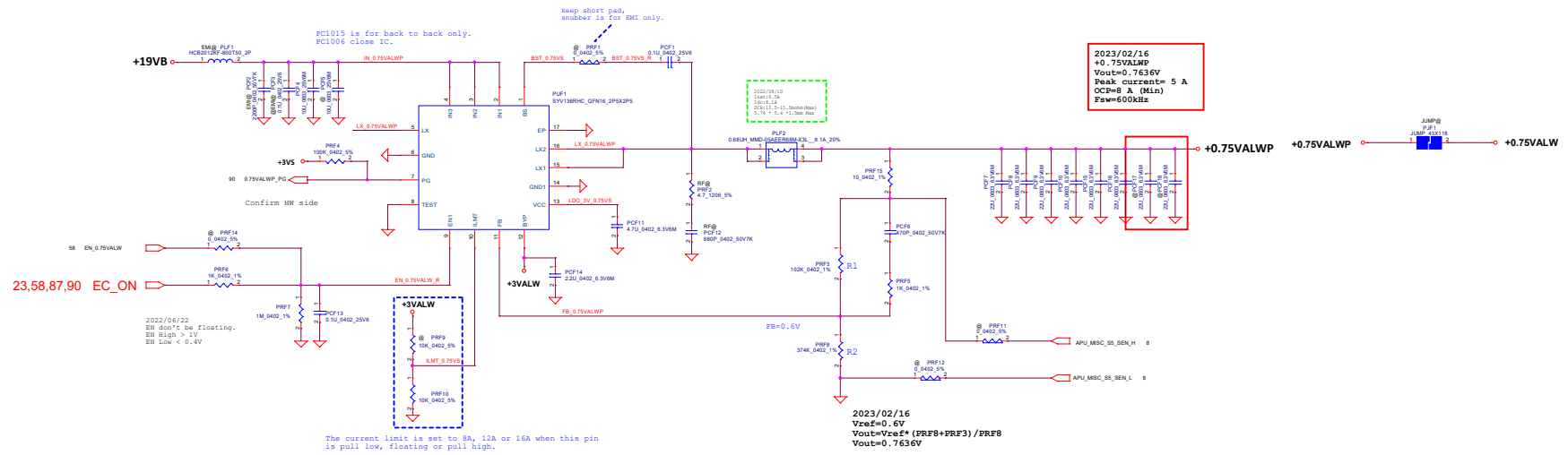


Module model information
BQ24780_V5.mdd for dual layer

Vin Detector		
	Min.	Typ
L-->H	17.16V	17.63V
H-->L	16.76V	17.22V

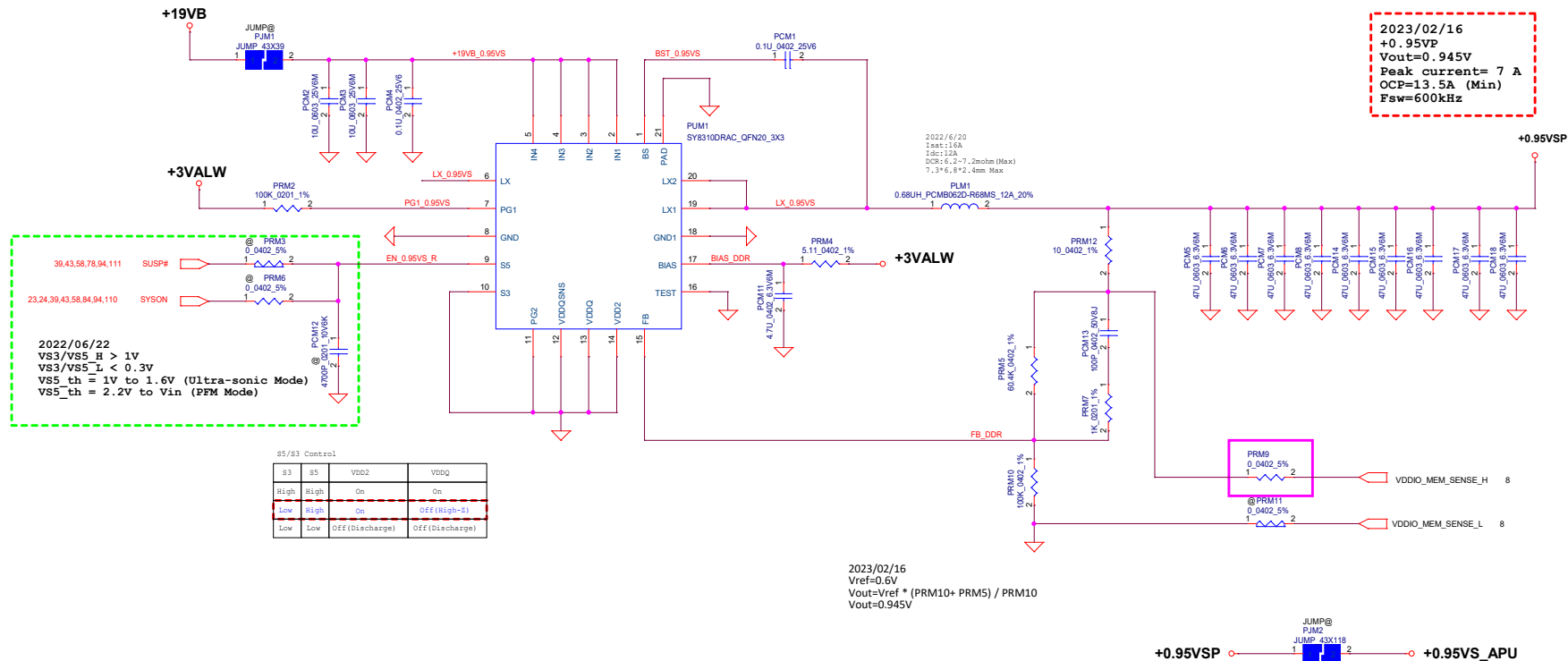
VILIM = 20 * IILIM * Rsr
IILIM = 3.3 * 100 / (316 + 100) / 20 / 0.01
= 3.966 A

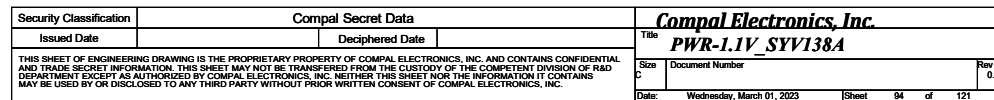
****Design Notes****
For 45 / 90W system, 381P/382P battery
Maximum Charging current 3A
Maximum Battery discharge power 55W
#Register Setting
1: Disable turbo when AC only
#Circuit Design
1. ILIM pull high voltage need base on 3/5W enable control
2. Use 7X7 choke and 3X3 R/L side MOSFET
Charge current: 3A
Power loss: 1.79W (H/s=0.22W, L/s=1.2738W, Choke=0.297W)
Power density: 0.45 (2X14)
#Protect function
1. ACOPV: VCC voltage > 24V
2. Charger timeout: No communication within 175s (default)
3. ADC: 3.3 X Input current DAC setting (default: Disable)
4. CHGOCV: based on charge current setting
5. BATOVF: 103-106V
6. BATLOW: 2.6V
7. TBRDT: 155C
8. TRADLT RT: 750mV (default: Disable)
9. TRADLT LOW: 230mV (default)



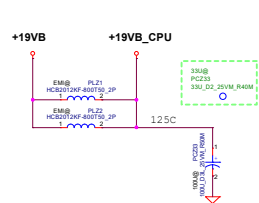
Please base on Vo ripple spec of your application to estimate output caps.

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		Date		Sheet	
		Wednesday, March 21, 2024		61	
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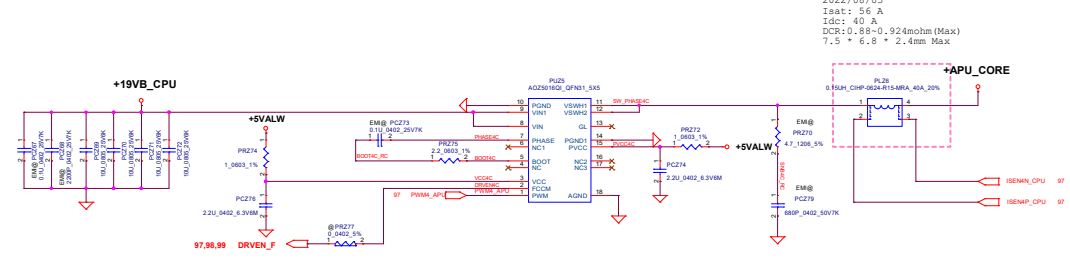
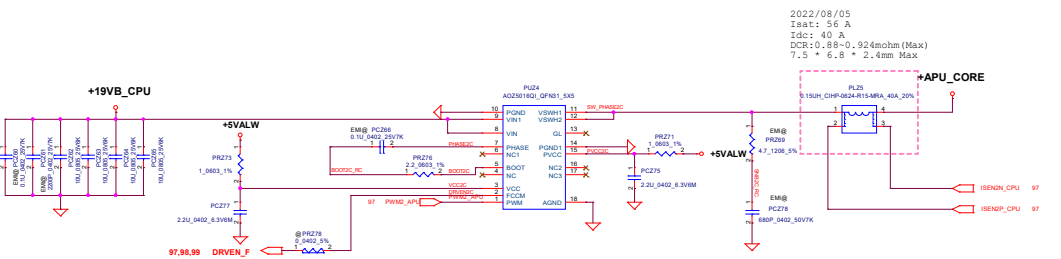
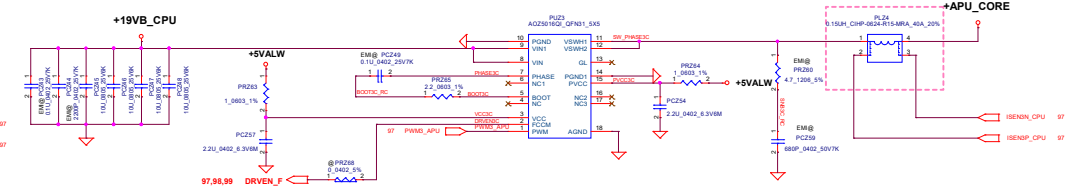
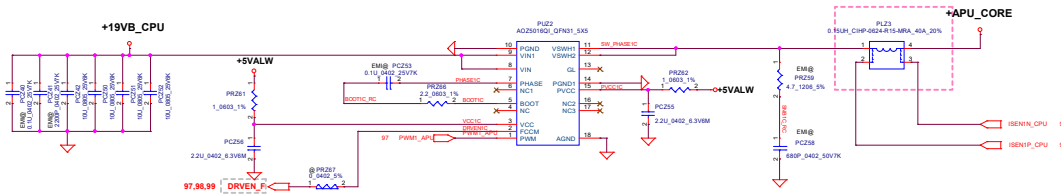


2022/06/27
+APU_CORE
ICCMAX=140 A
TDC=70 A
OCP=184 A
DC LL=0.3m ohm
AC LL=0.3m ohm

Switching Frequency= 600K Hz

2022/08/05
Isat: 56 A
Idc: 40 A
DCR: 0.88-0.924mohm (Max)
7.5 * 6.8 * 2.4mm Max

2022/08/05
Isat: 56 A
Idc: 40 A
DCR: 0.88-0.924mohm (Max)
7.5 * 6.8 * 2.4mm Max



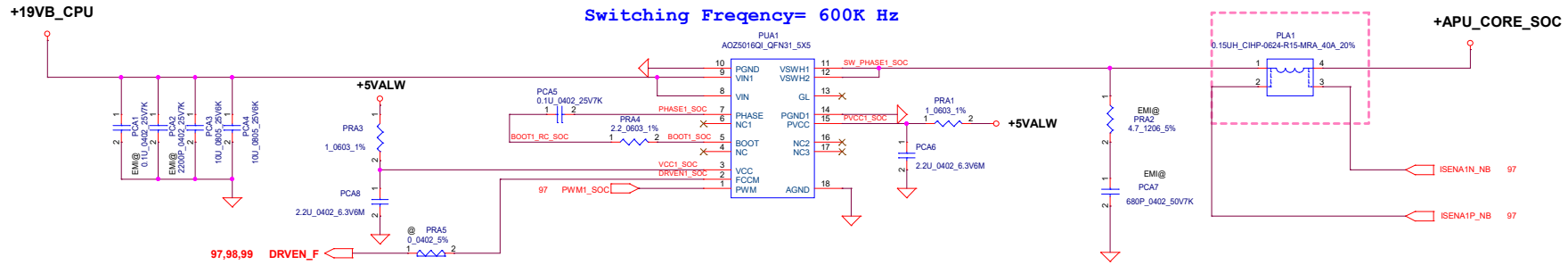
2CD:
SIC631= DRVEN
SIC632= DRVEN
SIC634= DRVEN
AO25038= DRVEN
FDMF3035= DRVEN
FDMF3037= DRVEN
FDMF5823= HighTHWn:
SIC631= Floating
SIC632= High
SIC634= Floating
AO25038= Floating
FDMF3035= Floating
FDMF3037= Floating
FDMF5823= High
DBI# :
SIC631= Floating
SIC632= High
SIC634= Floating
AO25038= Floating
FDMF3035= Floating
FDMF3037= Floating
FDMF5823= DRVEN

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2022/06/27
+APU_CORE_SOC

ICCMAX=26 A
TDC=18 A
OCP=32 A
DC LL=1m ohm
AC LL=1m ohm

2022/08/05
Isat: 56 A
Idc: 40 A
DCR: 0.88~0.924mohm(Max)
7.5 * 6.8 * 2.4mm Max

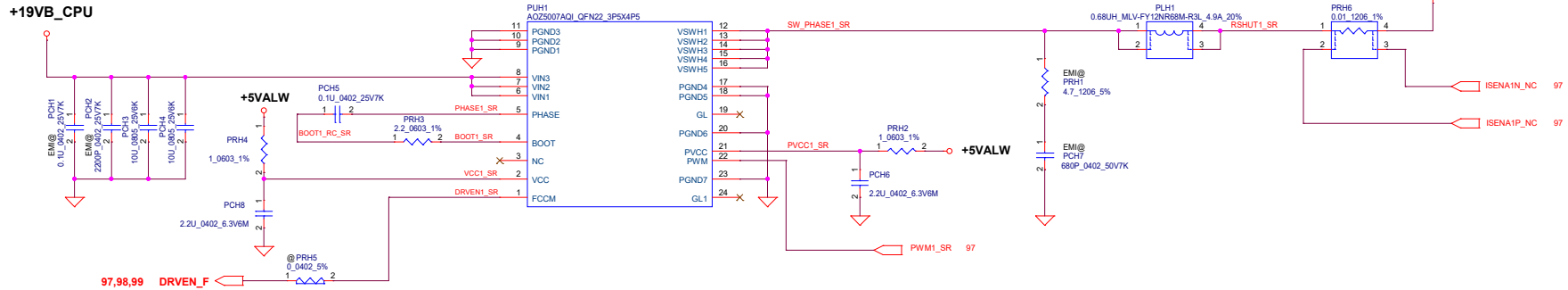


2022/06/27
+APU_CORE_SR

ICCMAX=3 A
TDC=2 A
OCP=6 A
DC LL=0m ohm
AC LL=0m ohm

Switching Frequency= 600K Hz

2022/08/05
Isat: 6A
Idc: 4.9 A
DCR: 21~26 mohm(Max)
3.4 * 2.7 * 1.2.0mm Max



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+APU_CORE

+APU_CORE

+APU_CORE_SOC

+APU_CORE_SOC

+APU_CORE_SOC

APU_CORE_SOC_2022/08/10
0.22uF*8
180pF*1
22uF*24
330uF*3(B2x2pcs, D3x1pcs)
330u is common part SGA00009S00

+APU_CORE_SR

+APU_CORE_SR
APU_CORE_SR_2022/08/10
1U * 2
22uF * 18/20

+APU_CORE_SR

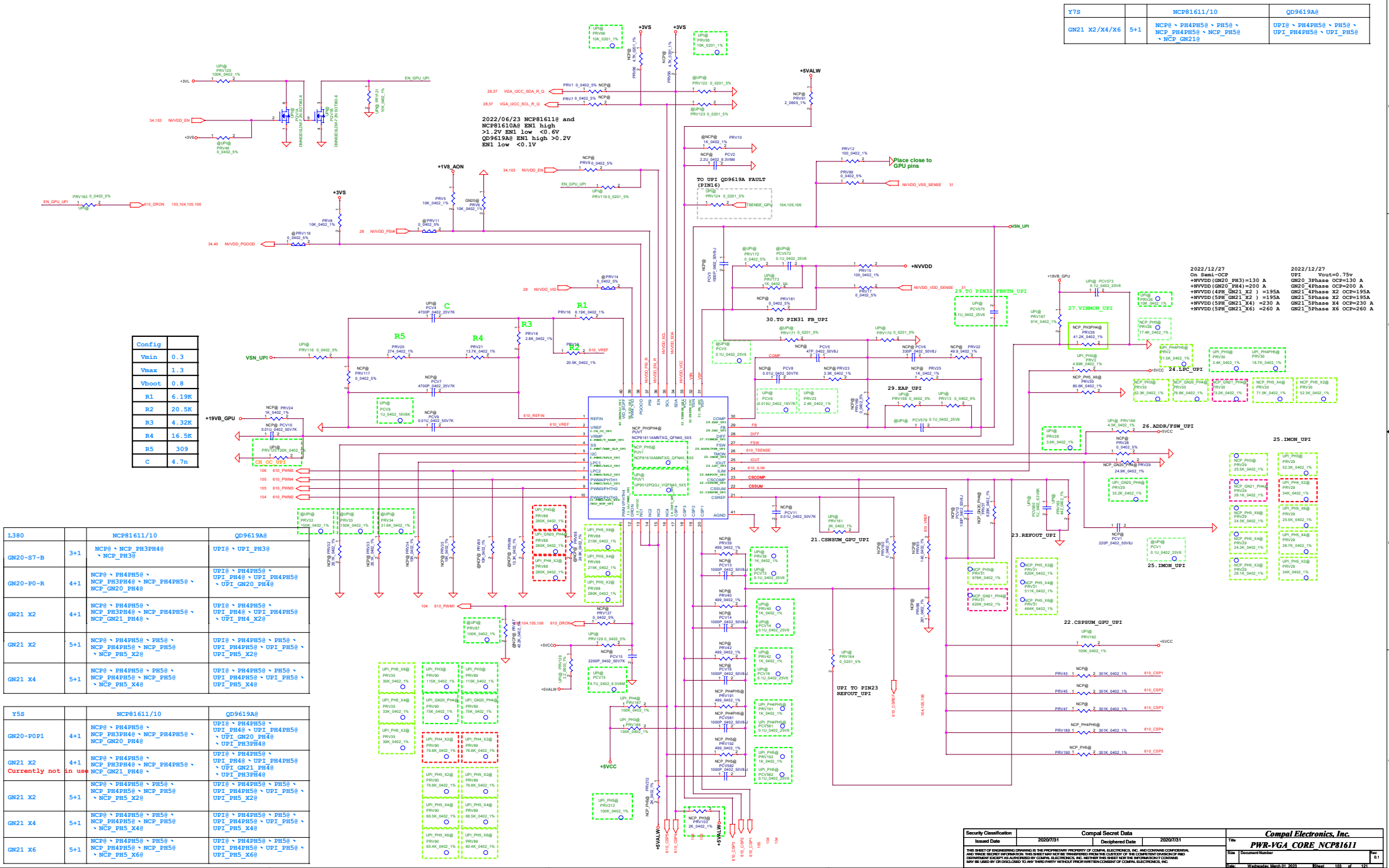
APU_CORE_2022/08/10
0.22uF*8
180pF*1
22uF*54
330uF(D3)*7
560uF(D1)*5

B2=1.9h, D3=1.4h, D7=1h
330u is common part SGA00006A00

Under CPU
Bot

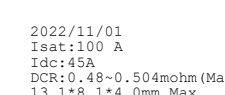
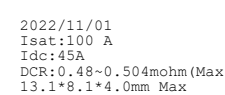
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Y78		NCP81611/10	QD9619A8
GN21 X2/X4/X6	5+1	NCP8 + PH4PH58 + PH58 + NCP PH4PH58 + NCP PH58 + NCP GN218	UPI8 + PH4PH58 + PH58 + UPI PH4PH58 + UPI PH58

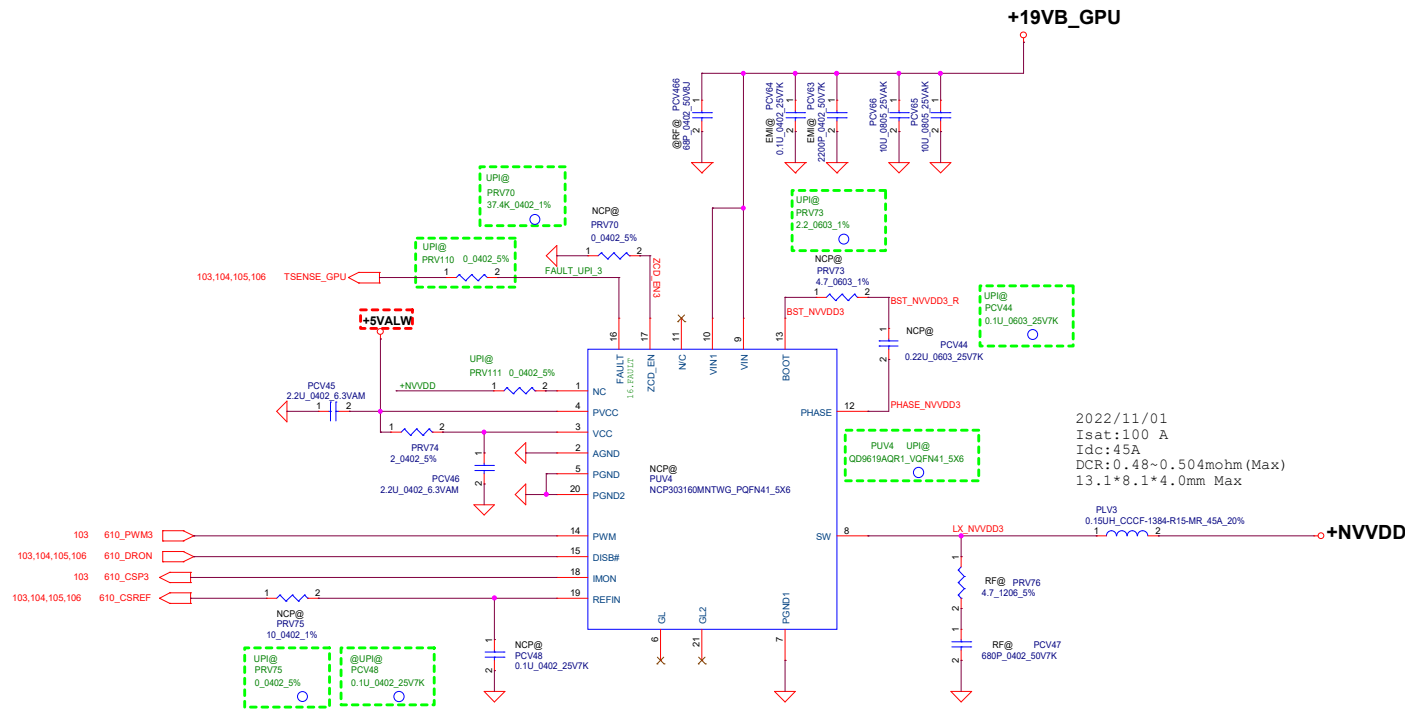


L380		NCP81611/10	QD9619A8
GN20-S7-B	3+1	NCP8 + NCP PH3PH48 + NCP PH38	UPI8 + UPI PH38
GN20-P0-R	4+1	NCP8 + PH4PH58 + NCP PH3PH48 + NCP PH4PH58 + NCP GN20 PH48	UPI8 + PH4PH58 + UPI PH48 + UPI PH4PH58 + UPI GN20 PH48
GN21 X2	4+1	NCP8 + PH4PH58 + NCP PH3PH48 + NCP PH4PH58 + NCP GN21 PH48	UPI8 + PH4PH58 + UPI PH48 + UPI PH4PH58 + UPI PH4 X28
GN21 X2	5+1	NCP8 + PH4PH58 + PH58 + NCP PH4PH58 + NCP PH58 + NCP PH5 X28	UPI8 + PH4PH58 + PH58 + UPI PH4PH58 + UPI PH58 + UPI PH5 X28
GN21 X4	5+1	NCP8 + PH4PH58 + PH58 + NCP PH4PH58 + NCP PH58 + NCP PH5 X48	UPI8 + PH4PH58 + PH58 + UPI PH4PH58 + UPI PH58 + UPI PH5 X48

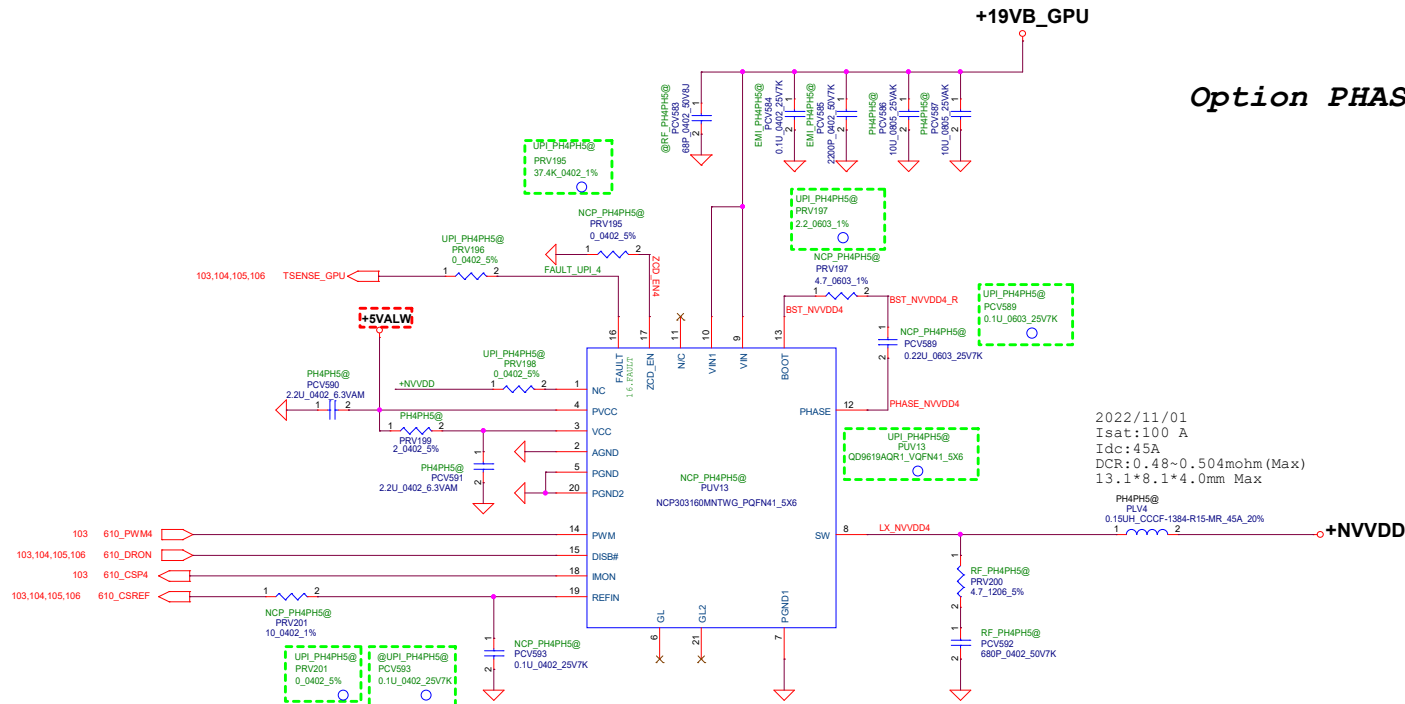
Y58		NCP81611/10	QD9619A8
GN20-P0P1	4+1	NCP8 + PH4PH58 + NCP PH3PH48 + NCP PH4PH58 + NCP GN20 PH48	UPI8 + PH4PH58 + UPI PH48 + UPI PH4PH58 + UPI GN20 PH48
GN21 X2	4+1	NCP8 + PH4PH58 + NCP PH3PH48 + NCP PH4PH58 + NCP GN21 PH48	UPI8 + PH4PH58 + UPI PH48 + UPI PH4PH58 + UPI PH3PH48
GN21 X2	5+1	NCP8 + PH4PH58 + PH58 + NCP PH4PH58 + NCP PH58 + NCP PH5 X28	UPI8 + PH4PH58 + PH58 + UPI PH4PH58 + UPI PH58 + UPI PH5 X28
GN21 X4	5+1	NCP8 + PH4PH58 + PH58 + NCP PH4PH58 + NCP PH58 + NCP PH5 X48	UPI8 + PH4PH58 + PH58 + UPI PH4PH58 + UPI PH58 + UPI PH5 X48
GN21 X6	5+1	NCP8 + PH4PH58 + PH58 + NCP PH4PH58 + NCP PH58 + NCP PH5 X68	UPI8 + PH4PH58 + PH58 + UPI PH4PH58 + UPI PH58 + UPI PH5 X68



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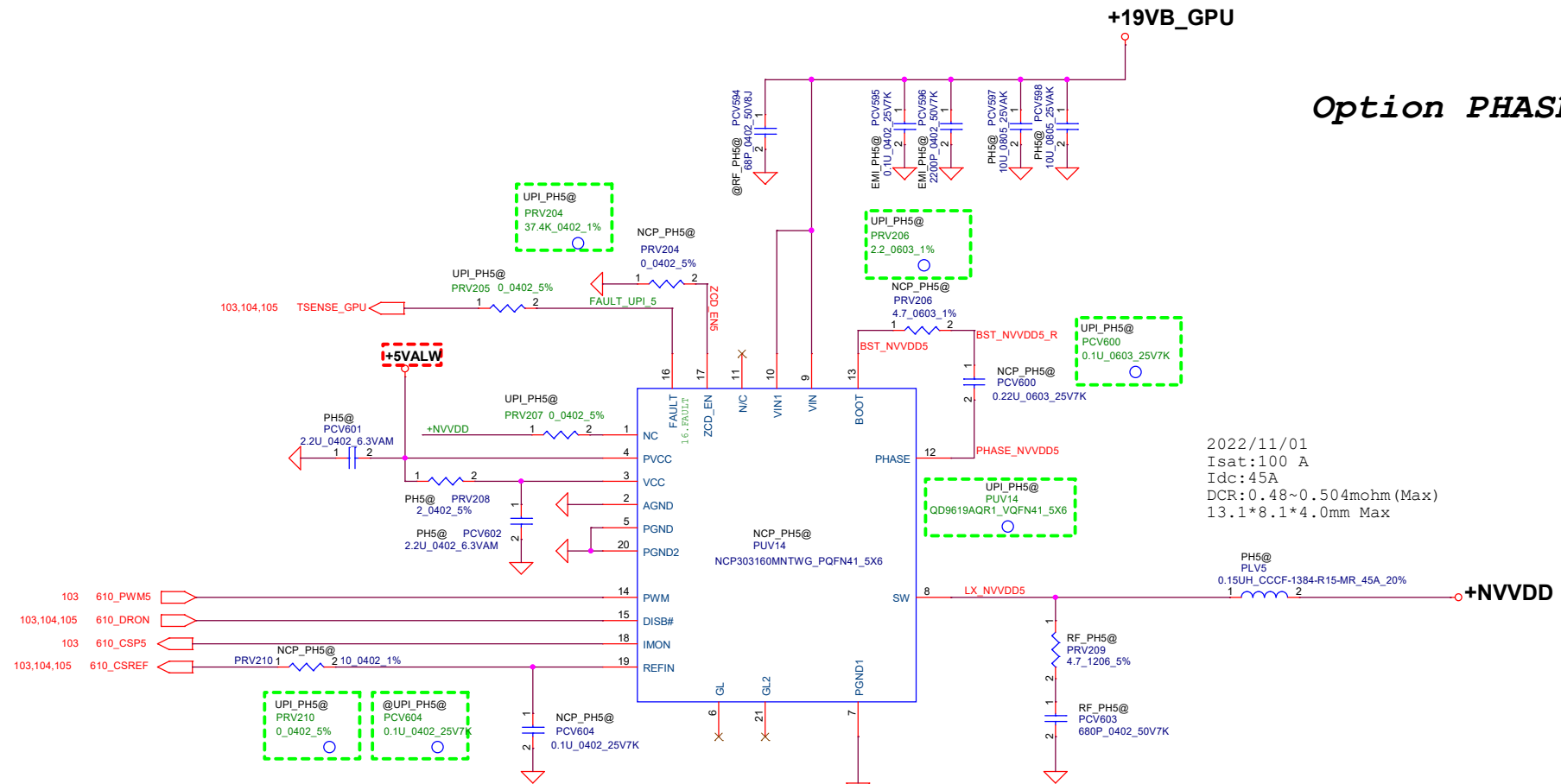


Option PHASE4



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Option PHASE5

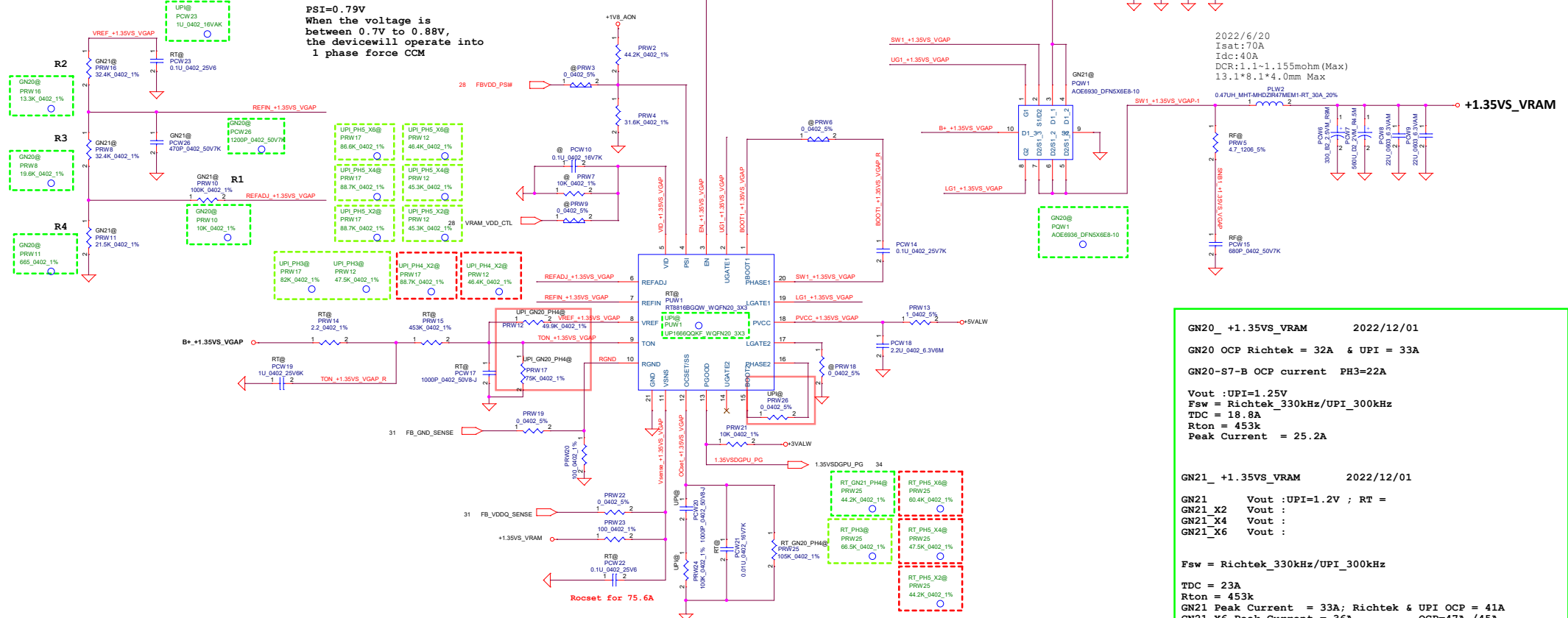


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2022/06/27
VPSI :
0V for 1Phase DCM
0.6V for 1Phase CCM

Samsung & Micron VRAM
When, VRAM VDD_CTL=High
Vboot=1.35V
When, VRAM VDD_CTL=Low
Vboot=1.25V

PSI=0.79V
When the voltage is
between 0.7V to 0.88V,
the device will operate into
1 phase force CCM



```
GN20_ +1.35VS_VRAM          2022/12/01

GN20 OCP Richtek = 32A  & UPI = 33A

GN20-S7-B OCP current  PH3=22A


Vout :UPI=1.25V
Fsw = Richtek_330kHz/UPI_300kHz
TDC = 18.8A
Rton = 453k
Peak Current  = 25.2A


GN21_ +1.35VS_VRAM          2022/12/01

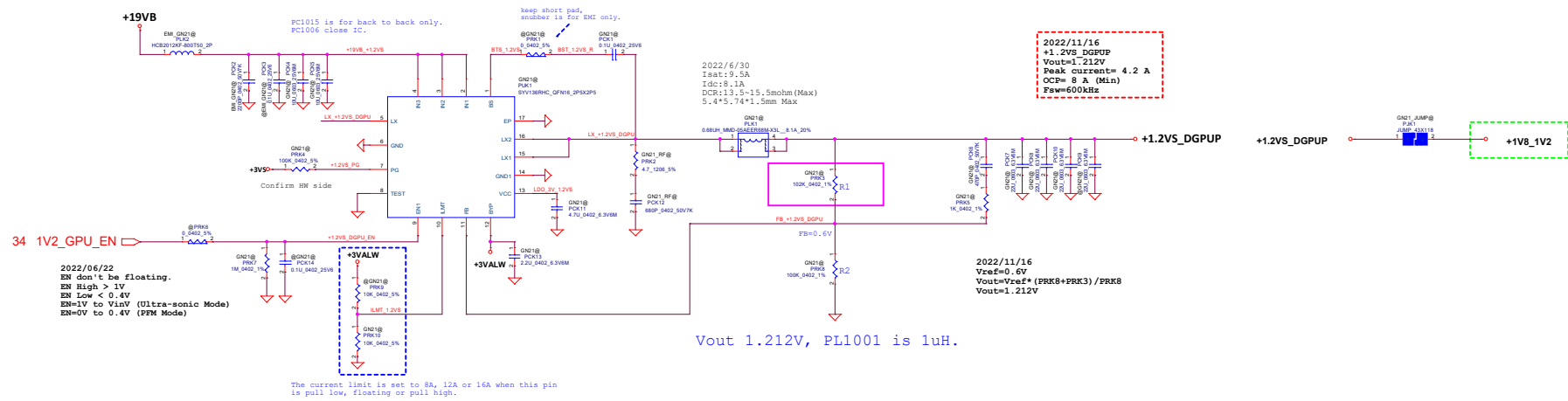
GN21          Vout :UPI=1.2V ; RT =
GN21_X2       Vout :
GN21_X4       Vout :
GN21_X6       Vout :

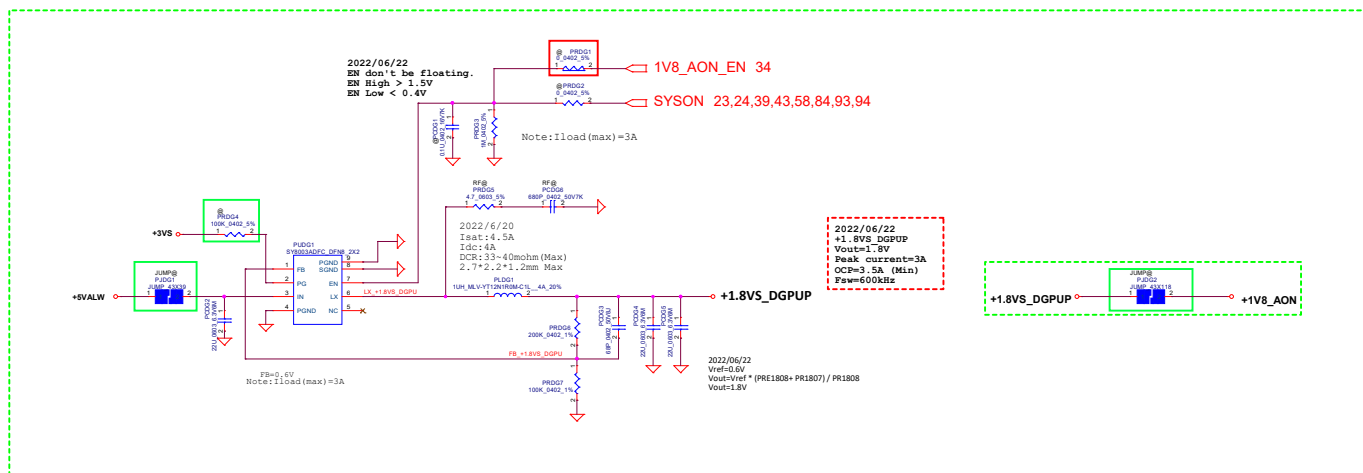
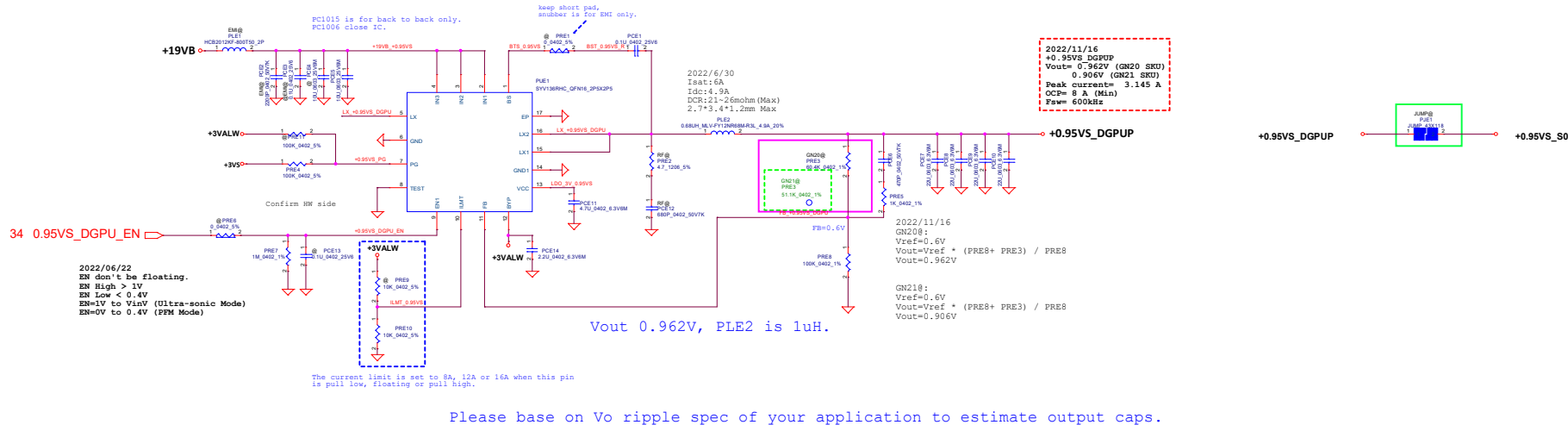

Fsw = Richtek_330kHz/UPI_300kHz


TDC = 23A
Rton = 453k
GN21 Peak Current  = 33A; Richtek & UPI OCP = 41A
GN21_X6 Peak Current = 36A          OCP=47A /45A
GN21_X4 Peak Current = 29A          OCP=38A /38.1A
GN21_X2 Peak Current = 27A          OCP=35A /38.1A
```

RT						UPI					
GN20-S7-B	GN20-P0-R	GN21_PH4	GN21_X2	GN21_X4	GN21_X6	GN20-S7-B	GN20-P0-R	GN21_PH4	GN21_X2	GN21_X4	GN21_X6
RTS 、 RT_PH3ø	RTS 、 RT_GN20_PH4ø	RTS 、 RT_GN21_PH4ø	RTS 、 RT_PH5_X2ø	RTS 、 RT_PH5_X4ø	RTS 、 RT_PH5_X6ø	GN20ø 、 UPI_PH3ø	GN20ø 、 UPI_GN20_PH4ø	GN21ø 、 UPI_PH4_X2ø	GN21ø 、 UPI_PH5_X2ø	GN21ø 、 UPI_PH5_X4ø	GN21ø 、 UPI_PH5_X6ø

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